Instrumentation

4000M System
Boeing Special Options
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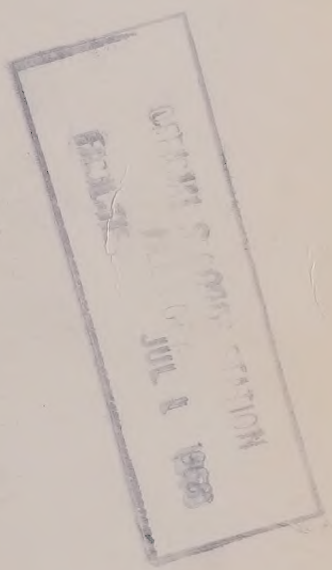

FAIRCHILD
INSTRUMENTATION

BOEING SYSTEM

SPECIAL DATA LOG OPTIONS

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SPECIAL DATA LOG OPTIONS

Several non-standard Data Log Options are included in the Boeing System.

The purpose of this paper is to explain the operation of each in turn. No explanation of Standard Fairchild Logic is provided, as the reader should have access to this information in another section of the manual.

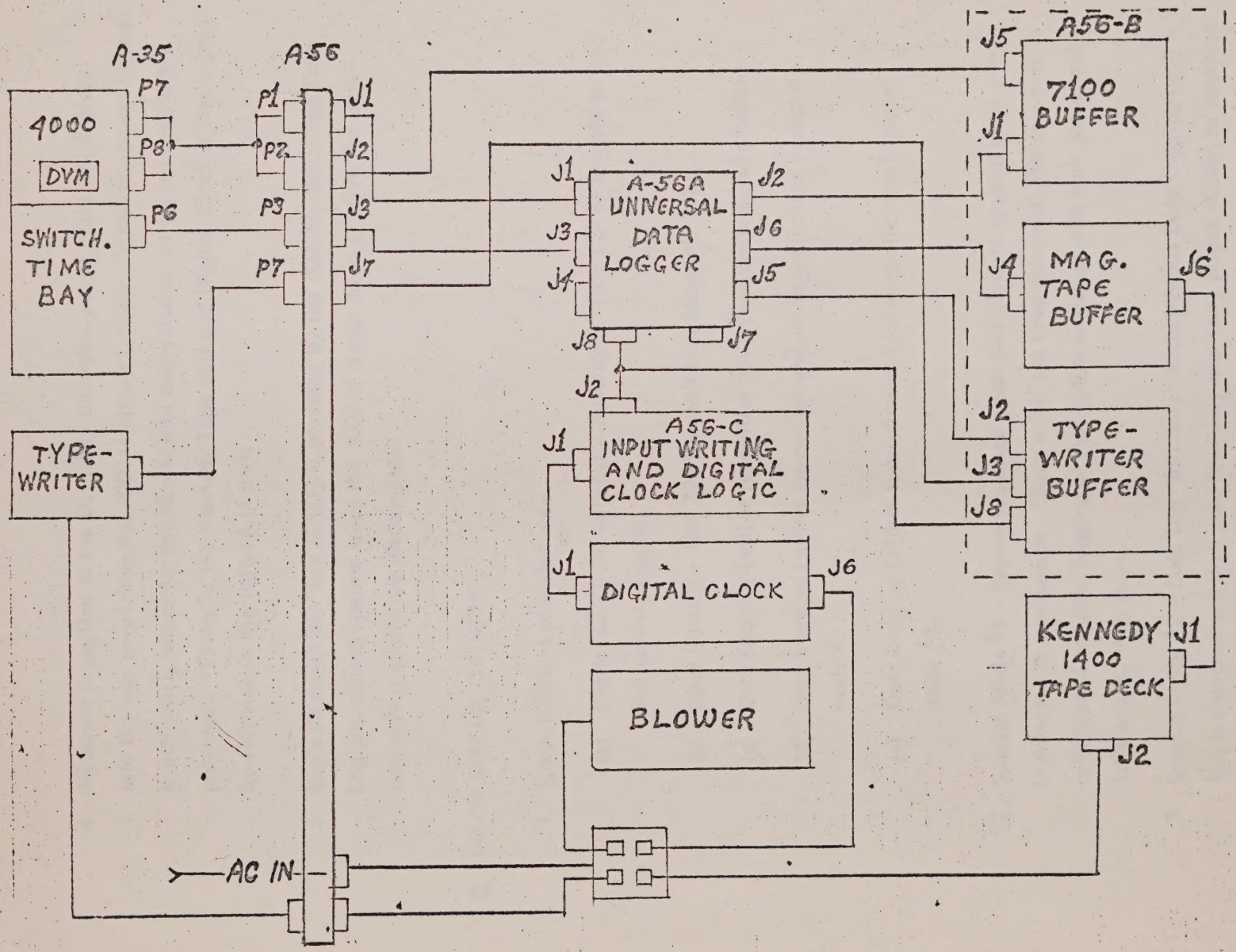
I. GENERAL DESCRIPTION

1. The phase number of the entire D.L. Bay is A56. All chassis in the Bay are designated by a further classification, denoted by a letter following this basic number i.e.,

   (a) Data Log Bay Phase Number — A56
   (b) Universal Data Log Chassis — A56-A
   (c) Composite Buffer — A56-B
   (d) Input Writing - Digital Clock Logic — A56-C
   (e) The actual Digital Clock & the Kennedy Tape unit are not given a number since they should be self-evident.

2. Figure 1 shows the internal cable connections of the Bay, as well as the external connections to the main 4000M; The Switching Time Bay; and the IBM 735 Typewriter.

3. Individual cable lists are provided for each cable in system coverage drawings, (a total of 8 pages) giving signal names on each pin when the pin is used for a signal. In most cases, the cables are of a 1 to 1 type. An obvious exception is the cable from the Input Writing-Digital Clock Logic Chassis (A56-C-P2) to the U.D.L. Chassis (A56-A-P8) & the Composite Buffer (A56-B-P8). This cable is of a "Y" split type.


A-35
A-56
A56-B
4000
DVM
SWITCH. TIME BAY
P7
P8
P6
P1
P2
P3
P7
J1
J2
J3
J7
J5
7100 BUFFER
J1
A-56A UNNERSAL DATA LOGGER
J1
J3
J4
J8
J2
J6
J5
J7
MAG. TAPE BUFFER
J4
J6
TYPE-WRITER
A56-C INPUT WRITING AND DIGITAL CLOCK LOGIC
J2
J1
TYPE-WRITER BUFFER
J2
J3
J8
DIGITAL CLOCK
J1
J6
KENNEDY 1400 TAPE DECK
J1
J2
BLOWER
AC IN

4. AC power is applied to the D.L. Bay through a power cable which plugs into the rear panel from the 4000 M circuit breaker. When the power breaker is activated, power for the blower and convenience outlets is immediately provided. (Power to the Kennedy Tape unit and Digital Clock is interrupted by switches on the individual units).

5. Logic Power (+30 V and GND) is provided by the 4000 M, hence the Data Log Bay cannot operate when the 4000 M is shut down or when the interconnecting cables are disconnected.

II. LIST OF SPECIAL OPTIONS

1. Special options provided are:

   (a) Digital Clock for automatic insertion of time (24 hr format) on each device data logged.

   (b) Input Writing - IBM 735 Typewriter to Magnetic Tape.

   (c) Data Logging (either typewriter and/or magnetic tape) standard.

   (d) Data Logging (either typewriter and/or magnetic tape) special mode #1.

   (e) Data Logging (either typewriter and/or magnetic tape) special mode #2.

2. Special Mode #1 - Repeat sequence mode inhibits data logging until a fail is detected in a sequence. Once a fail has been detected, the sequence is re-initiated and data logging of that entire sequence with both passes and fails occurs, then stops.

3. Special Mode #2 - Data Log "fail only" mode inhibits Data Logging until a fail is detected and then data logs only that test, allows 4000M to continue testing until next fail is detected, then again data logs that test only, and so on.

III. BLOCK DIAGRAM OF DATA LOG INFORMATION FLOW

1. To understand the special modes, it is necessary to have an overall picture of information flow within the entire system.

2. Referring again to Figure 1, we will take an example of the normal Data Log Mode; i.e., the printing of the DVM display on magnetic tape and/or the typewriter.

3. Assuming the system has been properly programmed and the necessary switches are in their proper positions, the following events occur:

   When the "TEST" switch of the 4000M is pressed, a "START" signal ($\overline{\text{STAR}}$) initiates a series of events in the U.D.L. (A56-A) which produces a "TAKE READING COMMAND" ($\overline{\text{STRC}}$) for the 4000M. Upon receipt of this signal, the DVM takes a reading and displays it, sending back a "PRINT COMMAND" (SPRC) to the U.D.L. (A56-A). The U.D.L. then clocks out the DVM information via the 7100 Buffer (A56-B) and the U.D.L. (A56-A) to the output device selected (through its Buffer); typewriter, or magnetic tape, or both simultaneously. Upon completion of the Data Logging, an "End of Word" signal ($\overline{\text{STST}}$) advances the 4000M to the next test; and the above sequence repeats until the end of the test sequence has been reached, at which all action stops. The signal that performs this function is appropriately named $\overline{\text{STOP}}$.

4. The data appears in the following format:

   (a) 4 digits of time information

   (b) 4 digits of serial number information (plus 2 digits for an identifier, when in MAGNETIC TAPE mode only)

(c) 1 digit of range, 4 digits of readout, one character of polarity, one character of Pass-Fail information. (plus one character for an identifier when in Magnetic Tape Mode.)

(d) The time and serial number are printed only once for a given sequence, and repeated only upon the initiation of another sequence.

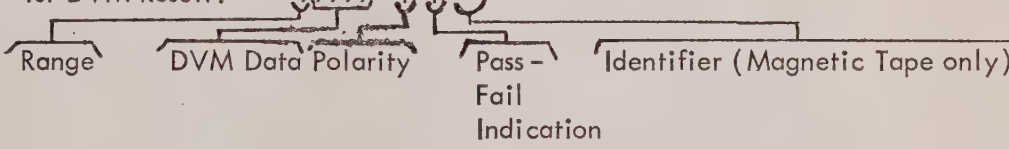
IV. TYPEWRITER MODE OPERATION

1. Conditions

(a) Time: 1234

(b) Ser. No: 5679 (XX) ------ Identifiers (Magnetic Tape only)

(c) 1st DVM Result: 99999 P P #



2. U.D.L. Front Panel Switches

(a)	026 Punch 526	Switch	Down	(Off)
(b)	Type	Switch	Up	(On)
(c)	Punch Tape	Switch	Down	(Off)
(d)	Magnetic Tape	Switch	Down	(Off)
(e)	Format	Switch	Pos. 7	(Selects word length)
(f)	Pol. Over Punch	Switch	Down	(Off)
(g)	Limit Over Punch	Switch	Down	(Off)
(h)	Ser. No.	Switch	Up	(On)
(i)	Sampling	Switch	Pos. 1	(Data Log all Tests)
(j)	Mode Select	Switch	Normal	
(k)	Input Writing	Switch	Off	
(l)	Power	Switch	On	
(m)	Ser. No. Display	05678		

3. Operation: (Assuming 4000M properly programmed)

A. 4000M reset button is pushed, producing a $\overline{\text{WRST}}$ Signal Resetting System and Data Log Bay.

B. 4000M Test button activated - producing a $\overline{\text{STAR}}$. $\overline{\text{STAR}}$ comes through the sampling rate switch on U.D.L. (A56-A) in its 1:1 position and is applied to 63FG4 which inverts it to a low signal. Since the position of the mode select switch (Normal) allows 62GB2 input K to be low, the output of this gate goes high, triggering the 100 μsec pulse, 25SDA2. SDSA remains set until the end test sequence or until the application of another manual reset.

C. At CD time, an $\overline{\text{STRC}}$ is produced at 46GC1, telling 4000M DVM to take a reading. When this has taken place, the U.D.L. receives a "Print Command" SPRC at 27GC4. When this signal arrives, the trailing edge fires the 50 μs one-shot 60SDA3 which sets the "Received Print Command" F/F - FBAN. (44GB1 & 2) FBAN remains set until completion of serial number sequence.

D. With FBAN set, a positive going level is seen at 43GC1 output "B" which, through the cables provided, is applied to the input-writing-digital clock chassis. (A56-C.) This level is inverted by 10FG1 and applied to one leg of a dual input gate. The other leg of this gate is wired through the digital clock normally open contacts of a switch to a fixed high level. The purpose of the switch is to inhibit further action if the clock is in a stepping process. Assuming the clock is not stepping, input "J" of 9GB2 is open (0 volts), a low at "K" allows the output "H" to go high triggering the 100 μsec one-shot 7SDA1, setting the clock ready-interrogate F/F, FCRI. This F/F remains until the time has been Data Logged.

E. At this point, several things happen simultaneously.

(1) $\overline{\text{FCRI}}$, the high level of the clock ready-interrogate F/F, is applied to 6GC2 in the U.D.L. chassis (A56-A) which removes the reset from the punch timing section of the U.D.L.

(2) At the same time, $\overline{\text{FCRI}}$ is applied to an input of 26GC4 in the IBM 735 Buffer section of the composite buffer, (A56-B); producing an STPP signal as a gate to R1, R2, R2A, R5, T1 and T2 signals to IBM 735.

(3) Going back to the U.D.L. (A56-A), with the reset removed, the punch timing section is in the SCO state awaiting a step from the typewriter. This SCO is connected to the input writing-digital clock chassis (A56-C) to 9GB3 input "H". The other input through an interlock in the clock (to prevent ambiguous readout during a clock step) is SCRI, the inverted $\overline{\text{FCRI}}$ signal. Since both signals are now low at 9GB3, its output goes high, through de-coupling diode CR1 into the clock chassis seeking out a closed contact in the hours (tens) stepper switch. Remembering from the "Conditions" paragraph this switch was in the "1" position, a high level appears at $\overline{\text{STAD1}}$ line (E2) in the clock chassis.

(4) $\overline{\text{STAD1}}$ is connected to the U.D.L. (A56-A) through the cables provided, to the "Decimal Decoded Drivers to Data Logging Buffers" - 39GCA2 input "K", providing an $\overline{\text{SBM1}}$.

(5) $\overline{\text{SBM1}}$ is applied to the composite buffer, IBM 735 typewriter section, to the Code Conversion Gates 35GC2, 35GC3, 35GC4 and 36GCB1, producing other necessary signal to "and" with STPP, thus enabling the correct relays to print a "1" on the typewriter.

(6) After printing the "1", a signal "COUNT" in the typewriter goes low, firing the O/S 28 SDA1 and producing a 40 msec pulse, the leading edge of which fires 28 SDA2, a 50 μsec one-shot (both in Typewriter Buffer of Composite Buffer, A56-B). 28 SDA2'S 50 μsec negative going pulse "ands" with SMTT (from U.D.L.) producing a positive going $\overline{\text{SEBI}}$, the trailing edge of 28 SDA2'S pulse fires another 50 μsec one-shot 28 SDA3, producing a positive going $\overline{\text{SECI}}$. $\overline{\text{SEBI}}$ performs no useful function at this time - however, keep in mind that it is produced after EACH character printed. $\overline{\text{SECI}}$, on the other hand, is now applied to the U.D.L. (A56-A) Punch Timing Section, producing a step to the counter, advancing it from SC0 to SC1.

(7) At SC1 time, in the Input Writing - Digital Clock Logic Chassis (A56-C), the hours (units) stepper in the clock is interrogated for its setting. (From "Conditions" Para. - this is a "2"). As before, this produces a $\overline{\text{STAD2}}$, producing an $\overline{\text{SBM2}}$ (in U.D.L.) which goes to A56-B Typewriter Buffer Section as an input to 35GC3, 35GC4, for code conversion. The proper relays are energized, the "2" is typed and the typewriter sends the typewriter buffer another "COUNT" pulse, producing another $\overline{\text{SEBI}}$ and $\overline{\text{SECI}}$ pulse. Again, as before, $\overline{\text{SEBI}}$ produces no useful action but $\overline{\text{SECI}}$ steps the counter in the U.D.L. from SC1 time to SC2 time.

(8) At this time it might be appropriate to interject a point. The reason a "1" was printed as the first character was because of the switch setting in the Digital Clock--not because it is in the first state of the Punch Timing Clock.

(9) To continue--at SC2 time, again in the Input Writing - Digital Clock Chassis (A56-C) the minutes (TENS) switch setting is read out, producing a pulse on the "3" line or $\overline{\text{STAD3}}$. $\overline{\text{STAD3}}$ produces an $\overline{\text{SBM3}}$ in the U.D.L. causing a "3" to be typed on the typewriter through the typewriter buffer (A56-B). Another "COUNT" is produced by the typewriter producing $\overline{\text{SEBI}}$ and $\overline{\text{SECI}}$ again.

(10) $\overline{\text{SECI}}$ again steps the Punch Timing Section in the U.D.L. to SC3 time. At SC3 time the minutes (units) switch setting is sensed and, as before, printed. However, on the trailing edge of SC3 time $\overline{\text{SCRC}}$ goes low, allowing the output of 10FG2 (in the Input Writing - Digital Clock Logic Chassis) to go high, firing 7SDA2 ($\overline{\text{SRMV}}$), a 1 msec one-shot which does several things, namely:

(a) First, it resets the FCRI F/F, applying a reset to the Punch Timing Section in the U.D.L. which returns to the reset or SC0 state.

(b) Simultaneously, it sets the 12GB3, 12GB4, F/F in A56-C.

(c) It also leaves the chassis - is connected to the Typewriter Buffer (A56-B) to 26GC1 input "F" forcing a "TAB" action by the typewriter.

NOTE: To prevent a commutation spike from prematurely firing 7 SDA3 in the A56-C and immediately stepping into the serial number mode, an 0.1μfd capacitor is placed on the input of 7 SDA3 to ground.

(11) With the TAB F/F in A56-B set, $\overline{\text{FTAB}}$ goes high, preventing the triggering of 7 SDA3 in A56-C until after the tab operation on the typewriter has been completed. ($\overline{\text{FCAR}}$ is also provided to prevent the possible initiation of serial NBR. printout during carriage return).

(12) When 7 SDA3 does fire, 12GB3, 12GB4 F/F is reset, and a 100μs pulse is cabled back to the U.D.L. and applied to the input of FSNU F/F 43GC3, 43GC4. This is the serial number F/F and it remains set until the 4 digits of serial number have been printed out.

(13) Once FSNU has been set low, the following events occur:

(a) $\overline{\text{FSNU}}$ goes high, lifting the reset from the Punch Timing Section in the U.D.L.

(b) $\overline{\text{FSNU}}$ is cabled to the IBM 735 buffer section of the composite buffer (A56-B) gating on the buffer via STPP exactly as $\overline{\text{FCRI}}$ did for the Digital Clock print-out.

(c) $\overline{\text{FSNU}}$ is inverted through 29 FG3 in the U.D.L. providing a gate for the SERIAL NUMBER DATA TIMING SIGNALS, $\overline{\text{SMCB}}$, $\overline{\text{SMCC}}$, $\overline{\text{SMCD}}$, $\overline{\text{SMCE}}$.

(14) Since the Punch Timing Counter is still in the SC0 state, $\overline{\text{SMCB}}$ goes high, interrogating the Most Significant Digit of the SERIAL NUMBER COUNTER. (From "Conditions" para. this is at a "5"). $\overline{\text{MCA5}}$ goes high, producing an $\overline{\text{SMB5}}$ which is cabled to the Typewriter Buffer Section of A56-B.

(15) $\overline{\text{SBM5}}$ is coded into the IBM format by the typewriter buffer, and a "5" is printed. Following the same procedure as was explained for the time print-out, $\overline{\text{SEBI}}$ & $\overline{\text{SECI}}$ are produced. (Disregard $\overline{\text{SEBI}}$ at this time, but bear in mind it occurs on every character). $\overline{\text{SECI}}$ steps the Punch Timing Counter in the U.D.L. from SC0 to SC1, producing a $\overline{\text{SMCC}}$ at 2 GB2 output of Serial Number Data Timing Counter, producing an $\overline{\text{MCA6}}$ which is printed as before.

(16) In a like manner, the remaining digits of Serial Number are printed out - "7" at SC2 time, and "8" at SC3 time.

(17) At SC3 time, the gate for the last Serial Number Character, $\overline{\text{SMCE}}$ goes high, and is applied not only to the Serial Number Counter, but also to 29 FG7, input "S" where it is inverted and "ANDED" with $\overline{\text{WMTM}}$ at 26GB3. Since both inputs are low, the output of this gate goes high. This high signal forces the output of 45GC3 low where it awaits the "Completion of Character Signal" $\overline{\text{SEBI}}$. When $\overline{\text{SEBI}}$ appears as an input to 45GC4, this high going pulse forces the output of 45GC4 to pulse low. 47GB4 output then goes high triggering 48SDA1 - SECP O/S, of 1 msec duration.

(18) $\overline{\text{SECP}}$ (a 1 mS positive pulse) is cabled to the typewriter buffer in A56-B, and used to reset the "FCLR" F/F, assuring that should a failure occur in the soon to be printed data, it will cause a "Red Ribbon Shift" on the typewriter allowing it to be printed in red for quick identification.

(19) SECP (a 1 msec low-going pulse) is "ANDed" with FSNU in A56-A, which is also still low at 47GB5. The output of this gate sets the "Punch Ready F/F" 55GC3 - 50GC1. FPUR goes low, and $\overline{\text{FPUR}}$ goes high.

(20) When $\overline{\text{FPUR}}$ goes high it triggers the $\overline{\text{SECQ}}$ one-shot 53SDA2, producing a 5 msec positive going pulse "$\overline{\text{SECQ}}$" and a 5 msec, low-going pulse "SECQ".

(21) "SECQ" is " anded " with "WTYP" to produce a high-going signal $\overline{\text{TTAB}}$ at 56GB3, which produces a TAB action on the typewriter to provide a space between Serial Number information and Data information. (The length of this space is determined mechanically by the typewriter. It can be as short as two spaces or as long as one line.)

(22) The positive-going trailing edge of SECP is used to fire 53SDA3, a 50μS one-shot. The positive-going pulse of this one-shot resets the FSNU F/F and takes us out of Serial NBR Mode.

(23) After the 5 msec one-shot $\overline{\text{SECQ}}$ has timed out, a positive-going pulse is seen at the input of 48SDA3, producing a 100μsec positive-going pulse $\overline{\text{SPRE}}$.

(24) $\overline{\text{SPRE}}$ resets FBAN F/F and sets FPUN the "Punch Mode" F/F.

(25) When FPUN goes low, it is " anded " with "WTYP" producing a high going signal $\overline{\text{TPUN}}$ at output of 47GB2.

(26) This $\overline{\text{TPUN}}$ produces a STPP in the typewriter buffer section of A56-B, just as $\overline{\text{FSNU}}$ did previously.

(27) $\overline{\text{FPUN}}$ is inverted at 29FG4 in U.D.L., producing a gate signal for the SC0 through SC7 timing signals. The " anding " of these signals produce new timing signals SC00 through SC07 in the "Test Results Data Timing" section of the U.D.L. Further, they produce, in sequence: SRAN, a low going "Range Gating" signal, "SDG1", "SDG2", "SDG3", "SDG4"; "DVM Result" gating signals, "SPOLA", a polarity gating signal and "SLIM" a Pass-Fail Gating signal.

(28) FBAN, F/F in the U.D.L. (A56-A) which was reset by $\overline{\text{SPRE}}$, is set thus: at CD time (from 4000 M) and an $\overline{\text{STRC}}$ (Take Reading Command) for the 4000 M is produced. After the DVM has reached its Display Mode, an "SPRC" or Print Command is received by the U.D.L., once again setting FBAN F/F.

(29) $\overline{\text{FPUR}}$ is used as an inhibit to prevent the output of 43GC1 going high-re-initiating the reading of the Digital Clock and Serial Number.

(30) At this time, the F/F's that are set are: SDSA, FBAN, FPUR and FPUN (FSNU is Reset.)

(31) With FPUN set, at SC00 time, an SRAN signal is produced, and depending on the Binary (1, 2, 4, 8) signals received from the 4000 M in the form of S061, S062, S064, S068, a range digit is produced by the range decoder. (From the "Conditions" paragraph this was to be a "9".) The range decoder provides an $\overline{\text{SAR9}}$, which in turn provides $\overline{\text{SBM9}}$.

(32) $\overline{\text{SBM9}}$ is cabled to the typewriter buffer section A56-B, producing a "9" on the typewriter.

(33) As before, $\overline{\text{SEBI}}$ and $\overline{\text{SECI}}$ are produced, $\overline{\text{SEBI}}$ to be ignored at this time, and $\overline{\text{SECI}}$ to step the Punch Timing Counter in the U.D.L.

(34) At "SC01 through SC04" time, the digits of the DVM are gated out via the 7100 Buffer section of the Composite Buffer A56-B. The digits are clocked out as binary (1, 2, 4, 2, *) and decoded into Decimal by the 11 DDD board in the 7100 Buffer. The $\overline{\text{DMV ( )}}$ information is then cabled back to the U.D.L. producing $\overline{\text{SBM ( )}}$ signals. Once this point has been reached, the typewriter buffer again accepts this data and a print-out is accomplished exactly as before.

(35) Polarity information cabled through the 7100 Buffer of A56-B (in the form of $\overline{\text{POLM}}$) from the 4000 M provides an indication of Positive or Negative to the U.D.L. $\overline{\text{POLM}}$ (and its inverse, POLM) determine whether a P or N is printed out at SPOLA time. (SC05 Time).

(36) At SC06 time, "SLIM" is generated which produces an $\overline{\text{SPAS}}$ or $\overline{\text{SFAI}}$ (Pass or Fail) as determined by STDT. STDT is the signal provided by 4000 M to indicate a fail condition; i.e., it goes low if a device has failed the test.

(37) $\overline{\text{SPAS}}$ produces a "P" on the typewriter, and $\overline{\text{SFAI}}$ produces an "F".

(38) When this last character (P or F) has been printed, another SECP is generated, resetting the FPUN F/F, and producing an $\overline{\text{STST}}$ at 49FG3 in the U.D.L.

(39) $\overline{\text{STST}}$ is used by the 4000M to step to the next test of the sequence where the whole data process is repeated.

(40) At the last test of a sequence, a $\overline{\text{STOP}}$ pulse is received from the 4000M, resetting the SDSA F/F, which in turn resets the FPUR F/F thru 53SDA1. (FPUN was reset by the last SECP pulse.)

(41) The system now awaits another start command from the operator; thus we have arrived at the conclusion of the last data logging step in the typewriter mode.

V MAGNETIC TAPE MODE

GENERAL:

1. In using the Kennedy Tape unit as a storage device for data obtained by the 4000M, you will note that the operation of the U.D.L. (A56-A) is quite similar to the operation as discussed for the typewriter mode.

2. The format is different only in the fact that 2 characters (as determined by the customer) are used to identify serial number information and 1 character (also determined by the customer) is used to identify data information on the tape. Identifiers are necessary in the tape mode as there is no seperation of data and Serial NBR on the tape as there is on the typewriter due to the fact that the typewriter can "TAB" and the tape unit cannot.

3. The general signal flow is from the 4000M to the U.D.L., to the Magnetic Tape Buffer section of A-56-B, and finally to the Kennedy Tape unit and onto the tape.

   CONDITIONS: As before with the exception that the typewriter switch is down, (OFF) and the Magnetic Tape switch is up or ON.

OPERATION:

1. As before, upon receipt of $\overline{\text{STAR}}$, SDSA F/F is set, generating an $\overline{\text{STRC}}$ at CD time. When SPRC is received by the U.D.L. again, FBAN F/F is set and a positive level will be observed at the output of 43GC1. This positive level, as before, initiates the interrogation of the Digital Clock setting.

2. $\overline{\text{FCRI}}$ goes high when FCRI F/F is set. $\overline{\text{FCRI}}$ removes the reset from the "Punch Timing" section of the U.D.L. and is cabled to the Magnetic Tape Buffer section of A56-B.

3. $\overline{\text{FCRI}}$ is applied to the input of 18EG7, and when it goes high the output goes low producing a low level at output of 2FG8. (FSPM goes low.)

4. When FSPM goes low, $\overline{\text{MTSCOS}}$ is already low, so both inputs of 14GB1 are low, allowing its output to go high.

5. 13GC3's output "N" goes low, and if we have a "Magnetic Tape Ready" signal ($\overline{\text{MTRR}}$ is high), DO NOT have an "End of Tape" signal ($\overline{\text{MTET}}$ is low) and "Mag Tape Broken" signal $\overline{\text{MTTB}}$ is low, the output of 13GC2 goes high and fires 12SDA1, a 100 μsec one-shot.

6. The trailing edge of this pulse triggers 12SDA2 a 10μsec adjustable one-shot that has been adjusted to exactly 10 μsec.

7. When 12SDA2 fires, a 10μsec positive-going pulse ($\overline{\text{MTSC1}}$) and a 10μsec negative-going pulse (MTSC1) are produced.

8. MTSC1 is used to gate out the first character of the clock. $\overline{\text{SBM1}}$ (produced from $\overline{\text{STAD1}}$) arrives from the U.D.L. and is converted to the 7 channel character "1" utilized by the Kennedy Tape unit. At MTSC1 time an output is observed at 15UG1; i.e., $\overline{\text{MTR1}}$ goes high.

9. $\overline{\text{MTR1}}$ cause a flux change to be recorded on the tape in the Kennedy unit.

10. Meanwhile, $\overline{\text{MTSC1}}$ going high has caused 9SDA1, an adjustable 1.8 msec to be triggered. The trailing edge of this pulse cause 10SDA1, a 2.2 msec one-shot to fire producing an $\overline{\text{SEBP}}$, which is similar to $\overline{\text{SEB1}}$, in that it has no significance at this time.

11. The trailing edge of the 2.2 msec pulse fires 11SDA2 producing a high-going 1 msec pulse $\overline{\text{MTSCOS}}$, and a low-going, 1 msec pulse MTSCOS simultaneously.

12. MTSCOS produces an $\overline{\text{SEPM}}$ at the output of 14GB2 which advances the Punch Timing Counter in the U.D.L., A56-A, to SC1 time.

13. $\overline{\text{MTSCOS}}$ goes high for 1 msec; and when it drops low again, the sequence is re-initiated by the positive pulse seen at the output of 14GB1.

14. This process repeats, character by character until SC3 time. (Or last digit from Digital Clock time).

15. At SC3 time, (SC3 goes low) and an $\overline{\text{SEBP}}$ occurs (at 10 SDA1 time in Magnetic Tape Buffer section), a positive pulse is seen at 8GC2 output in the Input Writing-Digital Clock logic chassis, A56-C.

16. This pulse resets the FCRI F/F in that chassis, removing us from the Digital Clock print-out mode.

17. Meanwhile, we have generated an output from 7SDA3, the 100μsec one-shot in the same manner as described for the Typewriter mode, except that now we do not have to wait for a "TAB" or "Carriage Return" action to be completed since we are not using the typewriter.

18. Once 7SDA3 fires, we initiate serial number mode by setting the FSNU F/F in the U.D.L. as before.

19. As before, the serial number counter is interrogated by the $\overline{\text{SMCB}}$, $\overline{\text{SMCC}}$, $\overline{\text{SMCD}}$ and $\overline{\text{SMCE}}$ signals, producing the proper inputs to produce $\overline{\text{SBM5}}$, $\overline{\text{SBM6}}$, $\overline{\text{SBM7}}$ and $\overline{\text{SBM8}}$ from the U.D.L.

20. These inputs are decoded by the Magnetic Tape Buffer section of A56-B, writing the proper digits on the tape (along with parity check on channel "C") as has been discussed for the clock print-out.

21. At SMCE time in the U.D.L. we do not produce an SECP as before, due to the fact that WMTM is high, inhibiting 26GB3.

22. Instead, at SC4 time and SC5 time, in the "Special Drivers to Data Logging Buffers" section, we produce a high going signal $\overline{\text{S358}}$ which is used to print an identifier of the customers own choosing.

23. The method for utilizing this is to cable $\overline{\text{S358}}$ to the Magnetic Tape Buffer section of A56-B and apply it to the inputs of the GC gates, card 3 & 4 necessary to make up the desired character.

24. Since there is no Flux check in this system, $\overline{\text{FFLX}}$ may be removed from the desired gates and $\overline{\text{S358}}$ substituted, providing there is no connection between the $\overline{\text{S358}}$ lines and the $\overline{\text{FFLX}}$ line on card 5. If this is done, no identifiers will be printed on the tape since the 2nd input to these gates will be high at SC4 and SC5 time, inhibiting any identifier desired. Further, "6T" must be disconnected.

25. NOTE - The 2 identifiers must be the same character.

26. Once the identifiers have been printed, we produce an SECP pulse to step us out of serial mode in the following manner:

    a. 45GC2 output in U.D.L. goes high at SC5 time providing a low input at 47GB4 - pin "R".

    b. Upon receipt of the last $\overline{\text{SEBP}}$ from the Magnetic Tape Buffer, Pin "S" of 47GB4 also goes low, allowing the output (Pin "P") to go high.

    c. When 47GB4's output goes high - it fires 48SDA1, giving us an SECP pulse and the action described in the typewriter section takes place, and we step from serial mode to data mode.

27. As previously described, the data is clocked out by the SC00 through SC07 signals, giving us range data at SC00 time.

28. At SC01 time DVM data is started through the 7100 buffer section of A56-B into the U.D.L. where it is converted to $\overline{\text{SBM ( )}}$ signals and cabled to the Magnetic Tape Buffer section of A56-B.

29. The Magnetic Tape Buffer re-converts this data to $\overline{\text{MTR ( )}}$ signals which are applied to the Kennedy Tape unit and written on the tape.

30. $\overline{\text{S358}}$ is produced by $\overline{\text{EMTW}}$ at the end of the first data word, via 61GC1.

The U.D.L. produces an $\overline{\text{SENM}}$ which goes to the Magnetic Tape Buffer as an "END OF DATA LOG WORD" signal. This produces an "END OF RECORD" signal $\overline{\text{MTGC}}$ which steps the tape 3/4" for End of Record Gap.

VI TYPEWRITER AND MAGNETIC TAPE DATA LOGGING

1. It is possible to use both the typewriter and the Magnetic Tape unit simultaneously.

2. The only difference is that the Magnetic Tape step command is then dependent upon the typewriter since it is the slower of the two.

3. In the U.D.L., under Print Command for Slaves, 54GC1's output goes high upon receipt of an STPP, producing an $\overline{\text{STPT}}$.

4. $\overline{\text{STPT}}$ then takes the place of SMMT in Magnetic Tape Buffer which is gated out by the typewriter switch $\overline{\text{WTYP}}$.

5. From then on, the action is as previously described, except that the $\overline{\text{SBM ( )}}$ data is applied to both buffers simultaneously, producing final data log outputs from both.

VII SPECIAL DATA LOG MODES

1. With a thorough understanding of how the previously described modes operate, the special modes are easy to explain.

2. Special Mode #1.

   a. The purpose of Special Mode #1 is to inhibit Data Logging as long as devices are passing all tests. As soon as a fail of any test in a sequence is detected, the 4000M is reset and restarted, and Data Logging of all tests in that sequence takes place.

   b. To accomplish the above, the "Mode Select" switch to the U.D.L. must be in the 2nd position, and the "Sampling" switch must be in the 1:1 position.

   c. 63FG1's grounded input produces a constant high output on the "Mode Select" switch swinger.

d. With a "High" on position 2, the output of 63FG2 is low, and $\overline{\text{FDLI}}$ is low, either from being manually reset ($\overline{\text{WRST}}$) or by the last received $\overline{\text{STOP}}$ pulse from the 4000M.

e. When a fail occurs, STDT goes low, and the output of 59GC4 goes high, firing the 1 msec one-shot 60SDA1. This pulse immediately resets the 4000M.

f. The trailing edge of this 1 msec pulse triggers 60SDA2, a 100 μsec one-shot which does 2 things:

(1) Sets FDLI (Data Log Inhibit) F/F. FDLI goes low and $\overline{\text{FDLI}}$ goes high, inhibiting the recycle path.

(2) It is also applied to an input on 61GC2.

g. FTOP F/F, 62GB5 and 6, was reset by the $\overline{\text{STAR}}$ signal when the "Test" button was depressed to initiate the sequence, so $\overline{\text{FTOP}}$ is low.

h. With $\overline{\text{FTOP}}$ low, the output of 61GC2 goes high when 60SDA2 fires, (for 100 μsec), producing a Restart Command to the 4000M.

i. When the 4000M restarts, another $\overline{\text{STAR}}$ is produced which follows its usual route in setting the SDSA F/F. It also sets FTOP F/F, causing $\overline{\text{FTOP}}$ to go high and inhibiting another Restart Command during this particular sequence.

j. Note: When FDLI F/F was set, $\overline{\text{FDLI}}$ went high, holding 62GB2's input "K" low - gating through $\overline{\text{STAR}}$.

k. Data Logging then occurs as previously described until the end of a test sequence has been reached and a $\overline{\text{STOP}}$ command is generated by the 4000M, taking the system out of the Data Log Mode.

3. Special Mode #2

a. The purpose of the Special Mode #2 is to data log failed tests only and to ignore the passes.

b. The "Mode Select" switch is in #3 position and the "Sampling" switch is in 1:1 position.

c. A constant high at 63FG1's output drives 63FG3's output low when in position #3.

d. When a fail occurs, STDT goes low allowing the output of 59GC2 to go high, firing 25SDA2 and setting the SDSA F/F.

e. Data Logging of time, Serial Number and failed test occurs; however, upon completion of the Data Log word the data logger awaits another "fail" signal (STDT). If no other fails occur, no further action occurs.

f. $\overline{\text{SSTC}}$ Produces the End of Data Log word: $\overline{\text{STST}}$.

g. The next detected STDT (fail signal) allows another data log action, as before except Time and Serial Number are not repeated.

VIII GLOSSARY OF LOGIC TERMS

This glossary is intended to supplement the glossary in the Model 4550 Data Log Module Manual, Table 5-1.

COUNT	Feedback signal from typewriter indicating completion of character.
DVM	General class of signals indicating DVM information.
EMTW	End of word signal in Magnetic Tape Mode.
$\overline{\text{FCAR}}$	Carriage return F/F signal.
$\overline{\text{FCLR}}$	Red Ribbon Shift printout enable signal.
$\overline{\text{FCRI}}$	Clock interrogate-ready signal, (from F/F).
$\overline{\text{FDLI}}$	Data-Log inhibit signal, (from F/F).
FFLX	Flux check F/F signal.
FSPM	Magnetic Tape Mode Data Log initiate signal.
$\overline{\text{FTAB}}$	Stops Data Logging until typewriter TAB operation is completed.
$\overline{\text{FTOP}}$	F/F indicating Data Logger has rcvd. a STOP pulse from 4000M.
$\overline{\text{MTET}}$	End of Tape signal.

$\overline{\text{MTGC}}$	100 μS Pos. pulse - produces "End of Record" in Kennedy. (Page 19).
$\overline{\text{MTRR}}$	Magnetic Tape ready signal.
$\overline{\text{MTSC}}$	Magnetic Tape Timing signals. (MTSC1, MTSC2, MTSCOS.)
SCRI	Inverted FCRI; Gate signal for interrogating Digital Clock.
7SDA1	Sets the clock-ready interrogate F/F.
SDSA	F/F which remembers that the 4000M produced a start signal.
$\overline{\text{SECQ}}$	Enable pulse (with WTYP) to produce TTAB.
$\overline{\text{SFAI}}$	Goes high on Fail; produces "F" on typewriter.
$\overline{\text{SMB (O)-(12)}}$	General class of signals indicating which decimal digit is to be Data Logged.
$\overline{\text{SPAS}}$	Goes high on pass - produces "P" on typewriter.
$\overline{\text{SPRC}}$	"Print" command.
SRMV	FCRI F/F reset; 12GB3, 12GB4 F/F reset typewriter "Tab" enable.
$\overline{\text{STAD (0)-(9)}}$	Digital Clock Data.

STDT	Fail condition signal.
$\overline{\text{STOP}}$	"Stop Action" command.
$\overline{\text{STRC}}$	"Take Reading" command.
$\overline{\text{STST}}$	"End of Word" signal.
$\overline{\text{S358}}$	Signal used to produce identifier in Magnetic Tape Mode.
$\overline{\text{TTAB}}$	Typewriter "TAB" signal to provide space between Ser. No. info & Data info.
$\overline{\text{WRST}}$	Signal for System reset.

4000M SYSTEM

60 LAMP TEST-FAIL OPTION

BOEING SPECIAL

4000M SYSTEM

60 LAMP TEST-FAIL OPTION

BOEING SPECIAL OPTION

The lamp check is enabled by programming a 99 on the TRACK SELECT switch and pushing the TEST button. The lamp-check signal BDIA sets all fail-lamp flip-flops so that all lamps illuminate when the TEST button is pushed. These lamps remain lit until the RESET button is pushed; this causes signal BRLD to be generated, deactivating all lamps.

The proper fail test lamp is illuminated by a signal from the test counter and the fail signal, BPDT.

The 20 FAIL LAMPS/60 FAIL LAMPS switch selects the number of fail lamps to be used. The "20 FAIL LAMPS" position enables the first 20 fail lamps to record the results of each track. The lamps are reset at the beginning of each track. The "60 FAIL LAMPS" position enables all sixty lamps to be used. The lamps display the results of the first three tracks in the test sequence, and are reset at the beginning of each test sequence.

4000M SYSTEM

200V V_f/I_f ADJUSTABLE CLAMP

BOEING SPECIAL OPTION

4000M SYSTEM
200 V V_f/I_f ADJUSTABLE CLAMP
BOEING SPECIAL OPTION

1. Description

The adjustable clamp is a clamp on the output voltage of the 200 volt V_f/I_f constant-voltage power supply. It operates only in the current forcing mode, and is disabled when a voltage is programmed. The clamp is adjusted manually by a knobpot on the front panel of the 200 volt V_f/I_f. There are two ranges: 0-100 volts, which is direct reading on the knobpot; and 0-200 volts (X2), on which the knobpot reading must be multiplied by two.

2. Operation

The clamp operates when the load voltage exceeds the reading on the knobpot. Any excess programmed current not flowing into the load will be sinked to ground. For example: If 100mA were programmed into a 10kΩ load, and the clamp set at 100 volts, only 10mA would be required by the load to give 100 volts, so there will be 90mA of excess current. This excess is sinked to ground through the clamp.

3. Theory of Operation

The schematic for the clamp circuit is shown in Figure 1. It is a modified Darlington with the second stage power transistors in parallel to share in the power dissipation. To see how the clamp works, consider the positive clamp. When the output voltage of the 200 volt V_f/I_f exceeds the voltage setting on the knobpot *(R6), Q1 gets turned on. This causes a voltage to be applied at the bases of Q2 and Q3, turning them on and providing a low resistance path to ground. If the output voltage of the 200 volt V_f/I_f drops below the clamp setting, Q1 ceases to conduct; which

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*NOTE: The Positive Clamp knobpot is R6 on the schematic and component locator; the Negative Clamp knobpot is R10.

brings the bases of Q2 and Q3 to ground, turning them off. Diode D1 serves two functions. It protects the base-emitter junction of Q1 from breakdown and, when the clamp is turned off, it prevents high leakage current from flowing throught Q1, Q2, and Q3.

4. Calibration Procedure for 200V V_f/I_f Variable Clamp.

1. Remove DVM input from rear connector and connect front input to pin 16 of test jig. 1.

2. Program +100mA range on 4000 for DPS 7 or DPS9 on test 1. Program -100mA range on test 2.

3. Program DPS 7 or DPS 9 to pin 16.

4. Connect 100KΩ load from pin 16 to ground.

5. Place X1 (0 - 100V) X2 (0 - 200V) switch in 0 - 200V position. Set variable clamp (Knobpots) to 10.

6. Adjust R4 for +200V in test 1. Adjust R5 to -200V in test 2.

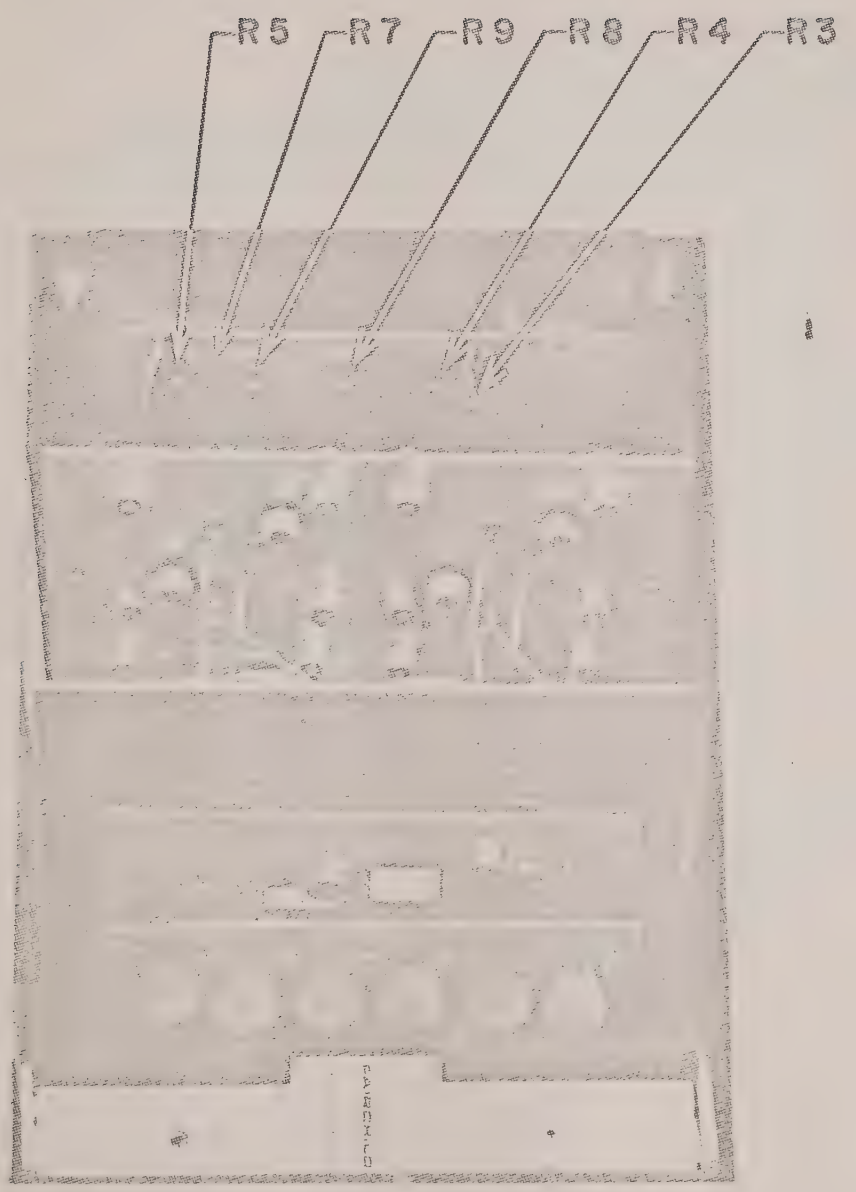
7. Switch ± clamps to X1 position. Adjust R8 for +100V in test 1 and R9 for -100V in test 2.

4000M SYSTEM
200V V_f/I_f ADJUSTABLE CLAMP

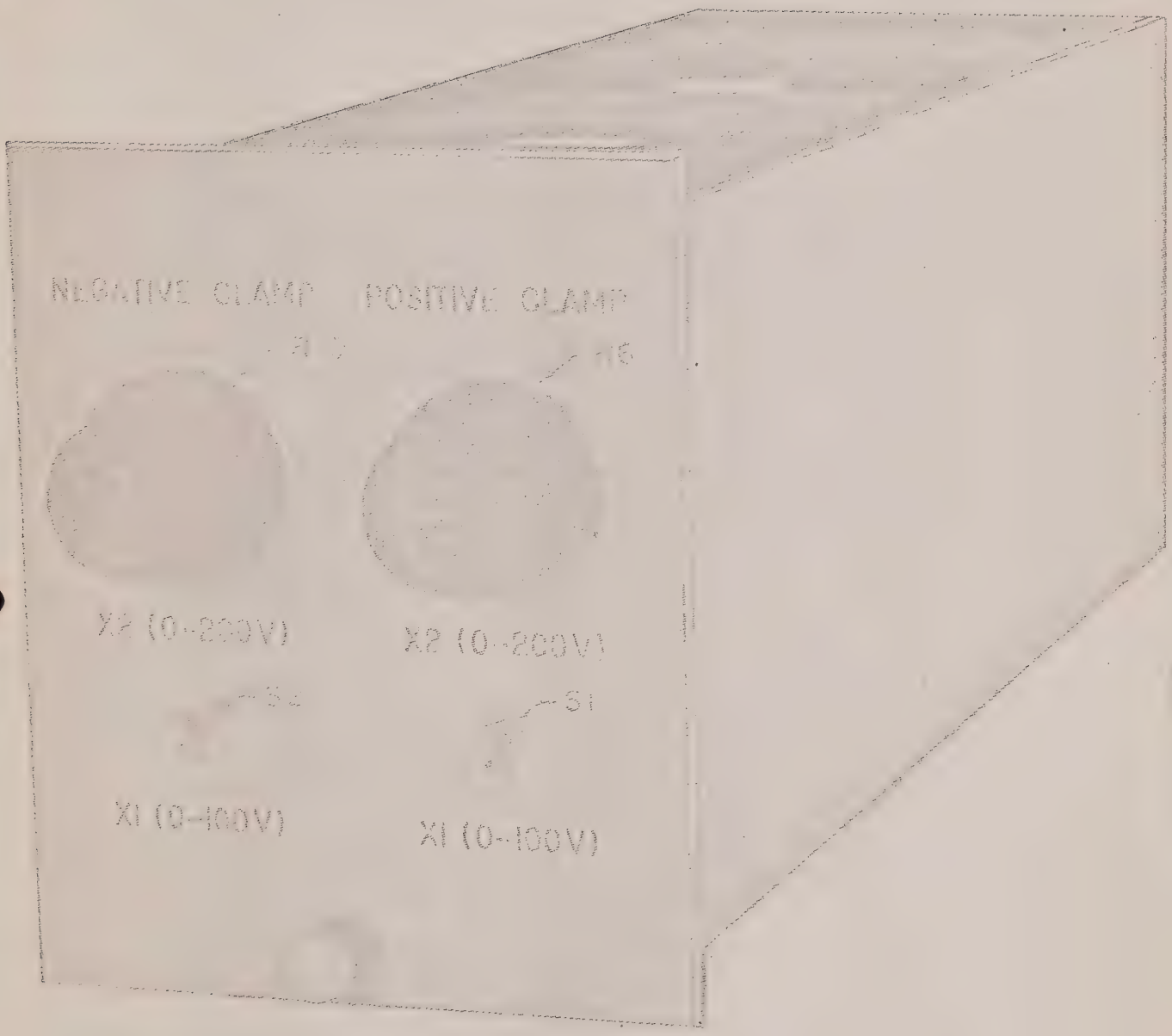
BOEING SPECIAL OPTION

Specifications

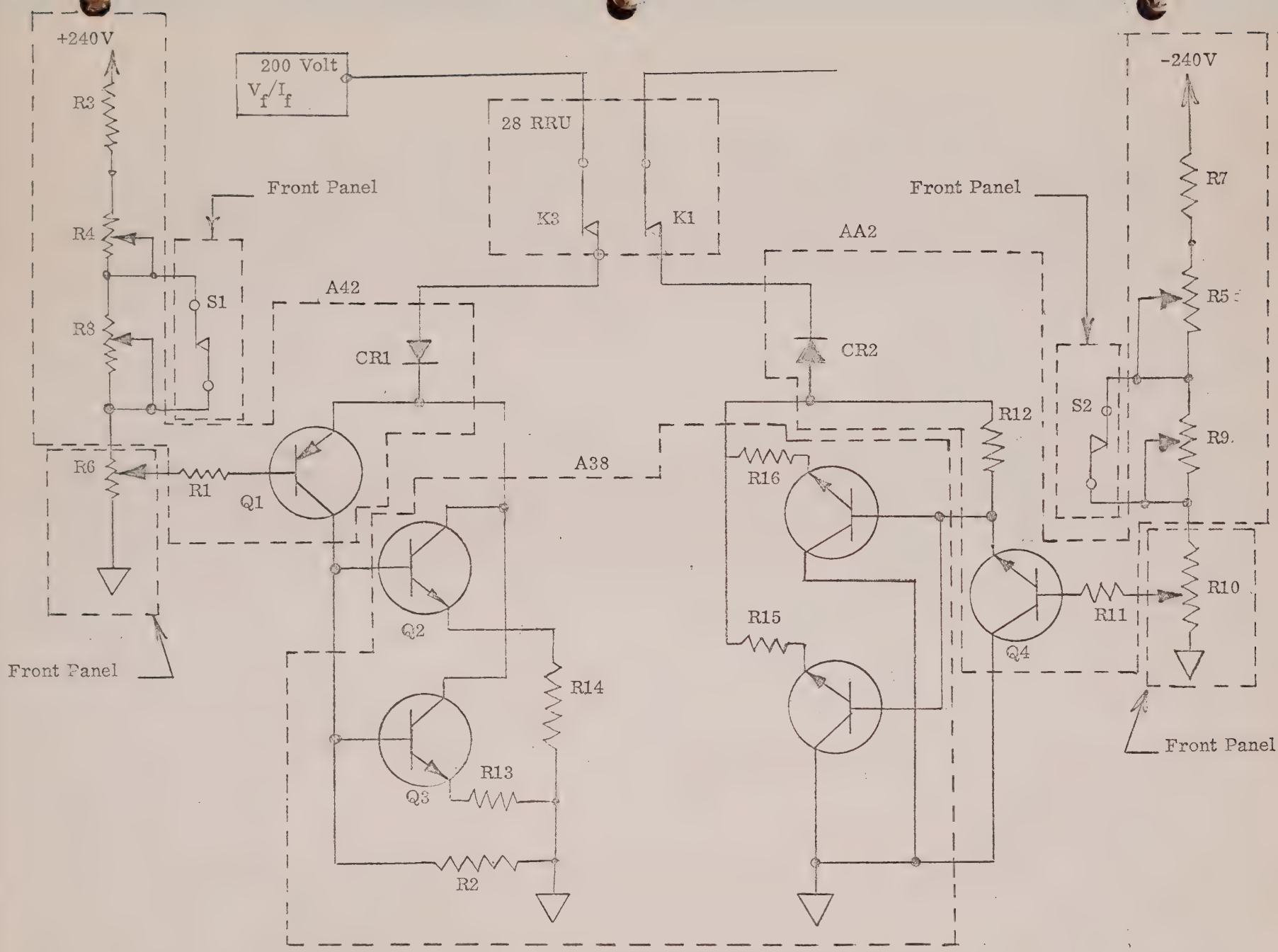
Accuracy:	±2% of Full Scale Range setting
Ranges:	0 to 100V 0 to 200V



RESISTOR LOCATION;
VARIABLE CLAMP
FOR 200 VOLT VF/IF



FRONT PANEL ;
VARIABLE CLAMP FOR
200 VOLT VF/IF



4000M SYSTEM - VARIABLE CLAMP (BOEING SPECIAL OPTION)

4000M SYSTEM

PULSER TO BE USED IN EXT. POS. #6

BOEING SPECIAL OPTION

4000M SYSTEM

PULSER TO BE USED IN EXT POS. #6

BOEING SPECIAL OPTION

1. VARIABLE OFFSET - VARIABLE AMPLITUDE PULSE
2. DELAYED CURRENT
3. LEVEL SHIFT TO GROUND
4. PROGRAMMING INSTRUCTIONS FOR CHARACTER 33

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1. VARIABLE OFFSET - VARIABLE AMPLITUDE PULSE - The Variable Amplitude Pulse is programmed by $\overline{U331}$ and by Matrix programming of Ext. Line 6. The pulse will appear concurrent with the first US04 signal and will have a width of 2.4 msec. The pulse output has a low output impedance capable of operating into load impedances as low as 50 Ω. Amplitude and offset are variable from 0 V to ±6 V; polarity is also selectable. Offset, amplitude, and polarity are set by front panel controls. $\overline{U331}$ · $\overline{U332}$ will allow a single pulse with offset until $\overline{U332}$ is reset, then it will drop back to 0 V. The Single Socket termination (50 Ω) should only be used in conjunction with the pulser under limited offset duty cycle limitations. The pulser is capable of ±6 V offset, thereby exceeding the 50 Ω 1/2 watt power rating at ambient temperatures. *

SPECIFICATIONS

(1.) Polarity	Positive or negative; manual select.
(2.) Amplitude	Adjustable; 0 to 6 V maximum Amplitude from 0 V reference.
(3.) Pulse width	2.4 msec, occurs after start of power pulse and before measurement.
(4.) Current rating	120 mA maximum source or sink.
(5.) Rise & fall time	1 μsec. maximum.
(6.) DC offset	Adjustable; 0 to ±6 V.
(7.) Boundary conditions	±6 V.

*See Next Page

Note that when "NEGATIVE" polarity is selected EXT Line 6 will step to the voltage level set by the "OFFSET" control at the beginning of the power pulse and drop for 2.4 msec at US04 time to a level equal to that set by the "OFFSET" control minus that set by the "AMPLITUDE" control. At the end of 2.4 msec the line will return to the level set by the "OFFSET" control.

On the other hand, when "POSITIVE" polarity is selected EXT Line 6 will step at the beginning of the power pulse to a voltage level equal to that set by the "OFFSET" control minus that set by the "AMPLITUDE" control, and at US04 time it will step to the level set by the "OFFSET" control for 2.4 msec. At the end of 2.4 msec the line will return to a level equal to that set by the "OFFSET" control minus that set by the "AMPLITUDE" control.

Refer to the pulser timing diagram for further clarification on the above.

SETUP PROCEDURE

The pulser has been designed to operate as explained above in order to allow the offset level and pulse amplitude to be accurately set by utilizing the voltage measuring capability of the 4000M system as follows:

A. Program a 1 in character 33 and a 6 in character 26. (This programs the pulser output on EXT 6 line to pin 16).

B. Program an 8 in character 57 (This connects the DVM to pin 16).

C. Place the 4000M system in continuous run mode with the "CONT Go/No-Go" switch and press start button.

D. Set the pulse "POLARITY" switch in the negative position.

E. The DVM will now continuously read the offset level from the pulser which may be adjusted to the desired value by the "OFFSET" control on the front panel of the pulser.

F. Set the pulse "POLARITY" switch in the positive position.

G. The DVM will now continuously read a voltage level equal to that set by the "OFFSET" control minus that set by the pulse "AMPLITUDE" control. The "AMPLITUDE" control may now be adjusted to obtain the desired pulse amplitude which will be equal to the reading obtained in "E" above minus that obtained in this step, ("negative polarity reading" - "positive polarity reading").

2. DELAYED CURRENT - DPS-7, a V_F-I_F or I_F supply, is programmed for either a positive or negative current by standard programming.

DPS-7 should not be programmed directly to the test head matrix. Program instead Ext. Line 4 to the desired device pin. Ext. Line 4 is connected to DPS-7 thru Ext. 6 box and is programmed by $\overline{U338}$. At US06 time, the relay completing the current source circuit closes and remains closed until completion of $\overline{BWDD}$. The compliance voltage is $\approx \pm 7$ V and test time should be 45 msec or longer. By programming $\overline{U332} \cdot \overline{U338}$, the constant current relays will remain closed until $\overline{U332}$ is reset.

3. LEVEL SHIFT TO GROUND - A Level Shift to Ground may be programmed to Ext. Line 5 by programming $\overline{U334}$. Ext. Line 5 is programmed to the desired device pin. The device pin is held at ≈ 3 V from $\overline{U334}$ time until US04; at that time, the output is switched to ground. Source resistance is $\approx$ 1.2K Ω . At the end of the power pulse, the output is open circuited. By programming $\overline{U332} \cdot \overline{U334}$, the output will remain at ground until $\overline{U332}$ is reset.

4. PROGRAMMING INSTRUCTIONS FOR CHARACTER 33

1 = Variable Amplitude Pulse - Pulse appears on Ext. 6 line at US04 time. Pulse width is 2.4 ms. Offset is concurrent with the power pulse (44.4ms). Pulse amplitude and polarity, as well as offset voltage absolute magnitude, are selected by controls on front panel of pulser.

3 = Same as 1 above except when using expanded word programming offset voltage will remain until DC register is cleared. (Rather than disappearing at end of power pulse).

4 = Level Shift to Ground - Programs approximately 3V to Ext. 5 line from start of power pulse until US04 time when the line is switched to ground until the end of the power pulse at which time the line opens.

5 = Combination of 1 and 4 above. Results in both a pulse to Ext. 6 line and a level shift to ground on Ext. 5 line.

6 = Same as 4 above except Ext. 5 line remains at ground when using extended word programming until DC register is cleared. (Rather than opening at end of power pulse).

7 = Combination of 1, 3, and 4 above. Results in both a pulse to Ext. 6 line with offset remaining and a level shift to ground on Ext. 5 line.

8 = Delayed Current - Connects output of constant current supply in DPS-7 position to Ext. 4 line from US06 time until end of power pulse at which time line opens.

9 = Combination of 1 and 8 above. Results in both a pulse to Ext. 6 line and delayed current to Ext. 4 line.

A = Same as 8 above except Ext. 4 line will remain connected to DPS-7 when using expanded word programming until DC register is cleared. (Rather than opening at end of power pulse).

B = Combination of 3 and A above. Results in pulse to Ext. 6 line and delayed current to Ext. 4 line with pulse offset and delayed current connection held until DC register is cleared when using expanded word programming.

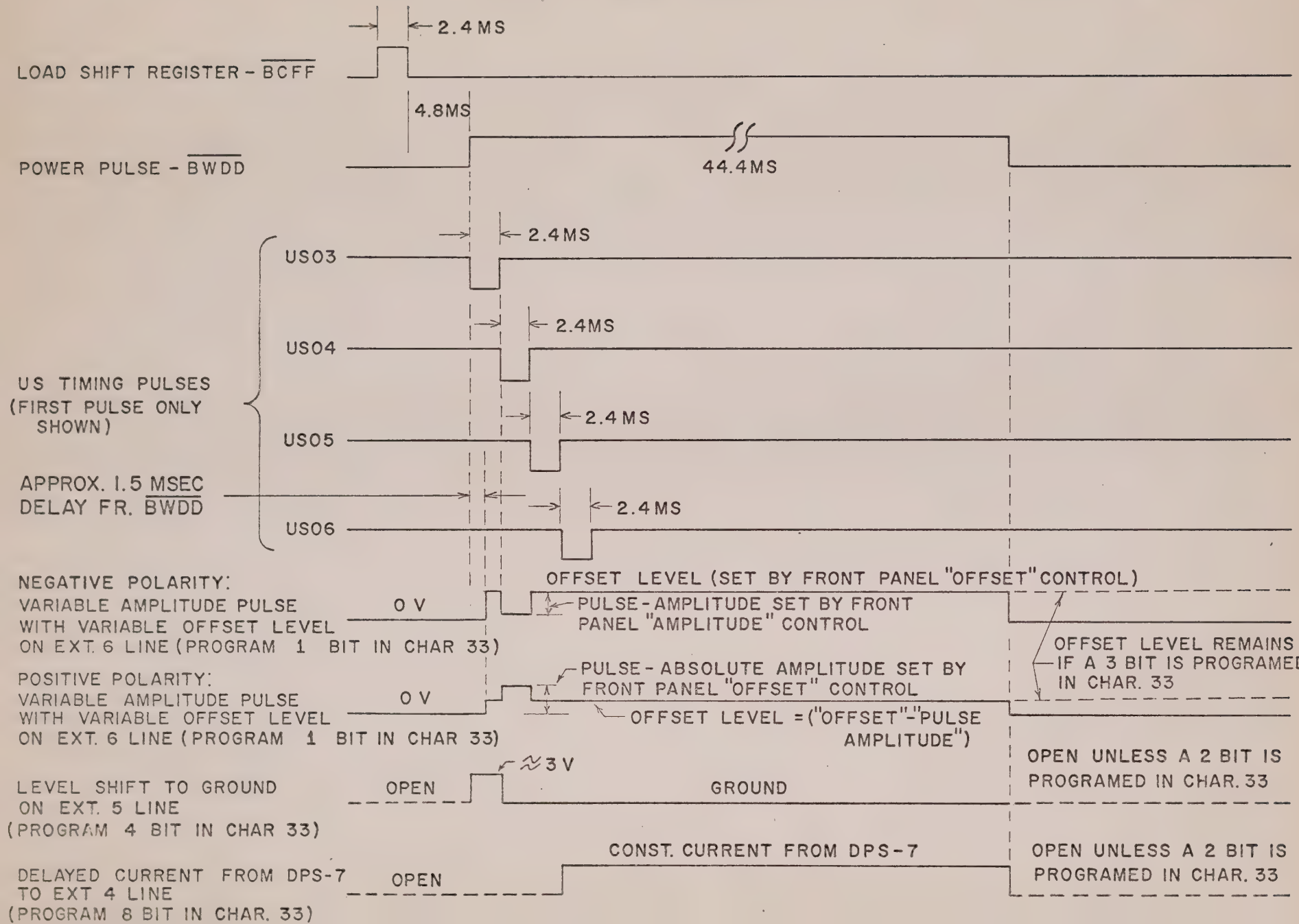
C = Combination of 4 and 8 above. Results in both level shift to ground on Ext. 5 line and delayed current on Ext. 4 line.

D = Combination of 1, 4, and 8 above. Results in pulse to Ext. 6 line, level shift to ground on Ext. 5 line, and delayed current to Ext. 4 line.

E = Same as 3 and A above. Results in pulse to Ext. 6 line and delayed current to Ext. 4 line with pulse offset and delayed current held until DC register is cleared when using expanded word programming.

F = Combination of 3, 6, and A above. Results in pulse to Ext. 6 line, level shift to ground on Ext. 5 line, and delayed current to Ext. 4 line with pulse offset on Ext. 6, ground on Ext. 5, and delayed current on Ext. 4 all held until DC register is cleared when using expanded word programming.

BOEING PULSER TIMING CHART


2.4 MS
LOAD SHIFT REGISTER - $\overline{BCFF}$
4.8MS
POWER PULSE - $\overline{BWDD}$
44.4MS
2.4MS
US03
2.4MS
US04
US TIMING PULSES (FIRST PULSE ONLY SHOWN)
2.4 MS
US05
APPROX. 1.5 MSEC DELAY FR. $\overline{BWDD}$
2.4 MS
US06
NEGATIVE POLARITY:
VARIABLE AMPLITUDE PULSE WITH VARIABLE OFFSET LEVEL ON EXT. 6 LINE (PROGRAM 1 BIT IN CHAR 33)
OFFSET LEVEL (SET BY FRONT PANEL "OFFSET" CONTROL)
0 V
PULSE-AMPLITUDE SET BY FRONT PANEL "AMPLITUDE" CONTROL
OFFSET LEVEL REMAINS IF A 3 BIT IS PROGRAMED IN CHAR. 33
POSITIVE POLARITY:
VARIABLE AMPLITUDE PULSE WITH VARIABLE OFFSET LEVEL ON EXT. 6 LINE (PROGRAM 1 BIT IN CHAR 33)
0 V
PULSE-ABSOLUTE AMPLITUDE SET BY FRONT PANEL "OFFSET" CONTROL
OFFSET LEVEL = ("OFFSET"-"PULSE AMPLITUDE")
≈3 V
LEVEL SHIFT TO GROUND ON EXT. 5 LINE (PROGRAM 4 BIT IN CHAR 33)
OPEN
GROUND
OPEN UNLESS A 2 BIT IS PROGRAMED IN CHAR. 33
CONST. CURRENT FROM DPS-7
DELAYED CURRENT FROM DPS-7 TO EXT 4 LINE (PROGRAM 8 BIT IN CHAR. 33)
OPEN
OPEN UNLESS A 2 BIT IS PROGRAMED IN CHAR. 33

4000M SYSTEM

DIGISWITCH MANUAL DELAY PROGRAMMER

BOEING SPECIAL OPTION

DIGISWITCH MANUAL DELAY PROGRAMMER

Remote - Internal Thumbwheel Switch Modification On EH Model 1420B Timing Unit

PROGRAMMING DELAY

The 1420B is a sub-assembly of the 4811 Pulse Generator. With the MAN-EXT SWITCH in EXT position, the delay is programmed from the magnetic disc. With the MAN-EXT Switch in the MAN position, delay is programmed with the 4-Segment Thumbwheel switch located on the front panel. Viewing the Timing Unit from the front panel, the left 3 segments are significant digits. Programming a zero in the first segment does not result in a calibrated value for the 2nd & 3rd Segments; therefore, a zero may not be used in the first segment. The fourth segment is a multiplier with positions programmed as follows:

External delay programming of Digiswitch Multiplier, fourth digit.

Programmed Digit	Multiplier	Range
0	uncalibrated	--------
1	10^{-1} nsec	10-99.9 nsec
2	10^{0} nsec	100-999 nsec
3	uncalibrated	--------
4	10^{-2} μsec	1-9.99 μsec
5	uncalibrated	--------
6	uncalibrated	--------
7	uncalibrated	--------
8	10^{-1} μsec	10-99.9 μsec

For example, setting the digit switch to 3121 would result in a delay of 312×10^{-1} nsec or 31.2 nsec. Setting the switch to 3124 would result in a delay of 312×10^{-2} μsec or 3.12 μsec.

4000M SYSTEM

AC GENERATOR

BOEING SPECIAL OPTION

AC GENERATOR OPTION, BOEING SPECIAL

A Wavetek AC Generator Model 155 is furnished with the Boeing 4000M. It is externally programmed from the Magnetic Disc via a program buffer. The program buffer logic tray is physically located in the 60 lamp panel logic chassis (Boeing system special). It receives data and register address information from the Magnetic Disc via the Control Logic logic tray in the DTVM bay.

The program buffer consists of a shift register and interface buffer circuits. The shift register is loaded with information programmed on the disc when word address 46 is programmed on the Magnetic Disc. The shift register outputs are connected to the buffer circuit inputs. The outputs of the buffer circuits are connected to the control lines in the Wavetek generator through a cable.

The Model 5800 DTVM instruction manual gives detailed instructions for programing the AC Generator. The Wavetek Model 155 instruction manual gives specifications on, and theory of operation of, the AC Generator.

4000M SYSTEM

LINEAR CIRCUIT OPTION FOR THE SINGLE SOCKET TEST HEAD

BOEING SPECIAL

ISSUED October, 1967

4000M SYSTEM

LINEAR CIRCUIT OPTION FOR THE SINGLE SOCKET TEST HEAD

BOEING SPECIAL

1. General Information

The Linear Circuit Option for the single socket goes into the slot for control card 20 inside the single socket test head (SSTH). It is designed to perform DC tests on the 702, 709, 710, and 711.

The Linear Circuit Option shown in Figure 1 is divided into two parts. The first is the linear circuit control card, which fits into slot 20 of the SSTH, and the second is the performance board for device under test (DUT). The linear circuit control card (LCCC) contains the common circuitry required by all devices. This includes a null amplifier, a sample and hold circuit, relays and precision scaling resistors. This same circuitry is used for every device type. The performance board is different for each device type and contains the circuitry required for the specific device under test. This circuitry includes the input resistors, frequency compensation, and load resistors.*

To see how each part of the linear circuit control card functions, consider the schematic of Figure 1. Relays K5, K6, K9, and K10 operate together and are enabled by programming a 4 in the 10th character of Word-Register 55. These relays are closed whenever it is desired to connect the null amp. around the DUT to null its output to zero.

Relay K1 is normally closed, and is opened by programming an 8 bit into the 10th character of Word-Register 55. K1 connects the output of the null amplifier to the input of the sample and hold amplifier. When it is desired to sample and hold

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*Control cards are required in slots 17, 18, and 19 for proper operation with the 702 sample performance board. These cards may be removed from slots 14, 15, and 16, since the cards in these positions are not used in the 702 program. The control connectors for these cards must be moved with the card to the associated receptacles; however, the co-ax lines to the 50Ω matrix can be left in their original place since they are not used in LIC tests.

the output of the null amplifier, relay K1 is programmed open, and the voltage is held on capacitor C1. The sample and hold amplifier is connected for unity gain, so that its output is the same as its input.

Relays K2, K3, and K4 operate together, and are closed by programming an 8 bit in character 5 of Word-Register 58. These relays are programmed closed whenever it is desired to apply the sample and hold voltage on the input of DUT. If K2, K3, K4, and K5, K6, K9, K10 are closed, K1 will always be programmed open.

Relays K7 and K8 are closed by programming a 1 and 2, respectively, in the 10th character of Word-Register 55. They are connected across the input resistors to the DUT, which are used to measure offset current. This will be described in detail in a later section.

2. Limitations in Testing Linear Circuits

There are some physical characteristics of linear circuits which introduce limitations in testing. The main limitation is that linear circuits have a finite warm-up time, during which their parameters (such as offset voltage and gain) will change. For example: If a 50msec test time is used to test a device and the results are compared with, say, a 2 second test time, the two readings can differ by as much as 40%. This is due to a higher degree of thermal stability being achieved with a 2-second test time.

Therefore, to obtain results comparable to those under which the linear circuit is to be used, the following procedure is recommended:

A. The first test of each test sequence should be at least one second (variable test-time option required).

B. Hold power between DTVM format tests. (Power goes off when DC register is addressed).

C. Use 50msec test times elsewhere, except in setup tests where relays are opened or closed, but do not affect stability of DUT or null amp. loop. These should be 8msec tests.

3. Description of DC Tests

The functions of the LCCC, performance board, and SSTH, and how they operate together to test linear circuits can best be described by considering a specific example.

Figure 2 contains the program sheets for a 702. They contain the programs to perform the following tests:

A. Input Offset Voltage
B. Input Offset Current
C. Open-Loop Voltage Gain
D. Common Mode Rejection Ratio
E. Input Bias Current
F. Power Consumption
G. Power Supply Rejection
H. Output Voltage Swing

The programs for each of these tests and how they are performed will be described separately.

A. Input Offset Voltage V_{os}

Definition: The input offset voltage is that voltage which must be applied between the input terminals to obtain zero output voltage.

Description of Test: Test 1 is a DC test in which +12 volts; -6 volts; ground; and the measuring line, are programmed to the appropriate control cards in the SSTH. Only one ground is programmed, and then it is bussed on the performance board to the appropriate points. The Go/No-Go limits are also programmed in this test. The time for this test is 1.0 sec, to allow the device to warm up.

Test 2 is a DTVM format test. During this test, the load relays for the DUT are programmed, as well as the relays on the LCCC.

Pins 2 and 3 are inputs of the 702. They are sensitive to capacitive loading, so the 8 bit is programmed to open the DC relays on these pins to reduce the capacitive loading. The same is true of pin 6, which is a compensation terminal. The junction of R5 and R6 is connected to ground through pin 19-1.

A 7 is programmed in character 10 of Word-Register 55. Since 7 is the numerical sum of the 1, 2, and 4 bits, relays K5, K6, K7, K8, K9, and K10 are closed. This connects the null amp. in a feedback configuration around the DUT, and shorts out the 2KΩ input resistors. The null amp. will null the output of the 702 to zero (see appendix). This implies the V_{os} is applied at the input of the 702. Since R4 and R5 form a 1000:1 attenuator, the output GNG limit programmed in test 1 is 6.5 volts, which is 1000 x V_{os} specification for a 702. Tests 3 and 4 repeat 1 and 2 with the negative sign on the GNG limit.

B. Input Offset Current

Definition: The input offset current is the difference in the currents into the two input terminals with the output held at zero volts.

Description of Test: Tests 1 and 2 are basic tests that will be performed repeatedly in the following tests when offset is to be nulled out prior to performing another test. For example, tests 5 through 8 are required to test for input offset current. Tests 5 and 6 are identical with tests 1 and 2 respectively, except the GNG limits have been changed. Tests 5 and 6, therefore, are used to null out the offset as a preliminary step in testing for offset current.

In test 7, relay K1 is opened by programming an 8 bit in word 55, character 10. Until K1 is opened, the input voltage of the sample and hold amplifier follows the output voltage of the null amp. (the time constant $R_{14}C_1$ is only 1.0 ms). When K1 is opened, this voltage is held on capacitor C1.

In test 8, an 8 bit is programmed in word 58, character 5, closing relays K2 and K3; this applies V_{os} to the input of the 702. The output of the null amp. would now be zero, except relays K7 and K8 are opened in test 8, which removes the short across the two 2K resistors at the input of the 702. The difference in

current flowing through these resistors (the offset current I_{os}) creates a differential voltage at the input of the 702, which is nulled out by the null amp. The voltage at the input of the 702 will be I_{os} (2KΩ). The output of the null amp. will be

$$V_{NA} = 1000\ I_{os}\ \ 2K\Omega$$

If V_{FM} is programmed to zero volts and connected to 18-1, the measured current will be

$$I_M = \frac{(1000)\ (I_{os})\ (2K\Omega)}{20K} = 100\ I_{os}$$

Test sequence 5, 6, and 7 is also used repeatedly, and will be referred to as sampling and holding the offset voltage.

Tests 9 through 12 are a repetition of tests 5 through 8, except the Go/No-Go limit is negative instead of positive.

C. Open-Loop Voltage Gain

Definition: Open-loop voltage gain the ratio of the change in output voltage to the change in voltage between the input terminals producing it.

Description of Test: The input offset voltage is sampled and held on the input of the DUT as in tests 5 through 7. This is done in tests 13 through 15, the only difference being that in test 13, DPS8 is programmed to 1 volt on pin 17. In test 16, load relay 1 of pin 17 is closed, connecting DPS8 to resistor R7. The null amp. loop is also opened in test 16.

Resistors R5 and R7 form a 1000 to 1 attenuator, making the DPS8 component of voltage on R5 equal to 1.0mV. This 1.0mV appears as a differential voltage between the inputs of the 702, and gets multiplied by the open loop gain of the 702. The output of the 702 will, therefore, be A_{vo}. (1.0mV), where A_{vo} is the open-loop voltage gain. In test 17, DPS8 is programmed to -1V, and the sample and hold option of the basic 4000 is utilized to hold the voltage of the previous test.

The result of test 17 will be A_{vo}(1mv) - A_{vo}(-1mv) = A_{vo} x 2 mv. The lower limit on the gain of a 702 is 1500. Therefore, the Go/No-Go limit for this test is 1500 x 2mV = 3.0 volts.

D. Common Mode Rejection Ratio

Definition: The common mode rejection ratio is equal to 20 Log $\frac{V_{cm}}{\Delta V_{os}}$, where V_{cm} is the common mode input voltage and ΔV_{os} is the differential input voltage required to bring the output to zero volts.

Description of Test: In tests 1 through 3 of the second program sheet, the input offset voltage is sampled and held on the input of the DUT. In test 4, the ground is removed from the junction of R5 and R6 by opening the utility relay on control card 19, and a V_{cm} of -4 volts is applied by closing load relay 1 on pin 19. Since the common mode voltage was programmed to pin 19 in test 1, it now appears at the junction of R5 and R6. In test 5, V_{cm} is changed to +0.5 volts and the result of test 4 is sampled and held in the basic 4000M.

The null amp. will null out the output of the DUT. Therefore, ΔV_{os} will be applied to the input of the DUT by the null amp. The output of the null amp. will be 1000 ΔV_{os}, and a Go/No-Go comparison is made on this voltage. The Go/No-Go limit is set for 1.42 volts and the common mode voltage is -4 and +0.5 volts. A pass implies a common mode rejection ratio of at least 70dB, from the following:

$$20 \log \frac{4.5}{1.42/1000} = 20 \log 3.16 \times 10^3 =$$

$$20\ (3.5)\ \text{db} = 70\text{db}$$

Tests 6 through 10 repeat tests 1 through 5, with the Go/No-Go sign reversed for ΔV_{os}.

E. Input Bias Current

Definition: The input bias current is the average of the two input currents.

Description of Test: In test 9, V_{FM} is programmed to zero volts on pin 19. In test 10, load relay 1 of pin 19 is closed, connecting V_{FM} to the junction of R5 and R6. The current measured is actually 2 I_B, so the Go/No-Go limit is programmed to 2 I_B. Another set of tests for the opposite sign is not required here, since the polarity of the bias current is known (conventional current flow is into the 702).

F. Power Consumption

Definition: The DC power required to operate the amplifier with the output at zero and with no load current.

Description of Test: This test is performed by programming V_{FM} as +Vcc and then as -Vcc, measuring the current in each test. Go/No-Go limits are placed on the current, since it is directly proportional to the power dissipation. When measuring power consumption, the offset is nulled out so that there is no load current. This is done in tests 1 through 4 of the third program sheet.

G. Power Supply Rejection Ratio

Definition: Power supply rejection ratio is the ratio of the change in input offset voltage to the total change in power supply voltage. It is generally expressed in μV/V (microvolts/volt).

Description of Test: With +Vcc at - 12 volts and -Vcc at - 6 volts, null out the offset voltage and sample and hold it on the input as shown in tests 5 through 7 of the third program sheet. Now change +Vcc to +6 volts and -Vcc to -3 volts, with the null amp. loop closed as in test 8. The output of the null amp. will be $V_{NA} = 1000\ \Delta V_{os}$. The total change in the power supply voltage is 9 volts. Hence, if $\Delta V_{os} = 2.7$mV, the power supply rejection is:

$$\frac{\Delta V_{os}}{9 \text{ volts}} = \frac{2.7\text{mV}}{9 \text{ volts}} = 300\mu\text{V/V}$$

The appropriate Go/No-Go limit is $1000\ \Delta V_{os} = 2.7$ volts. Tests 5 through 8 are repeated in tests 9 through 12, with the Go/No-Go limits reversed on ΔV_{os}.

H. Output Voltage Swing

Definition: Output voltage swing is the peak output swing referred to zero that can be obtained without clipping.

Description of Test: Null out, sample and hold offset voltage on input of DUT as in tests 13 through 15. With null amp. loop open, in test 16 apply +10 volts to R7 in order to saturate the DUT, and measure the negative output swing. In tests 17 through 20, repeat with opposite polarity. Go/No-Go limits of ±5 volts are placed on output voltage.

4000M SYSTEM

LINEAR CIRCUIT OPTION - SINGLE SOCKET TEST HEAD

BOEING SPECIAL

Programming information valid when LCCC is in Slot 20 of SSTH.

General Information

1. Always program a 0 in a character if the character is not used.
2. The instruction programmed in character 00 is used to control the format of the next test.
3. Format control is not available during a function test; the next test will always be addressed to the DC register.
4. The instruction programmed in character 09 is executed at the end of the next power pulse.
5. A "D" is always programmed in character 10. This is used as a register self-check.

Word-Register 55

Character No.	Function	Program
Tenth	Closes Relay K7 around input resistor R15 of DUT.	1
	Closes Relay K8 around input resistor R16 of DUT.	2
	Inserts Null Amp. in Feed-back configuration around DUT.	4
	Opens Sample and Hold Relay K1 to hold output voltage of Null Amp.	8

4000M SYSTEM

LINEAR CIRCUIT OPTION - SINGLE SOCKET TEST HEAD

BOEING SPECIAL

Programming information valid when LCCC is in Slot 20 of SSTH.

Word-Register 58

Character No.	Function	Program
Fifth	Connects output of Sample and Hold Amplifier to input of DUT. Also connects input voltage to DUT for gain and output voltage swing tests.	8

4000M SYSTEM
LINEAR CIRCUIT OPTION - SINGLE SOCKET TEST HEAD

BOEING SPECIAL
APPENDIX

The output voltage of the DUT (702) is given by

$$V_o = A_{vo} (V_p - V_I - V_{os}) \tag{1}$$

Where A_{vo} is the open loop gain, V_p is the voltage on the non-inverting input, V_I the voltage on the inverting input, and V_{os} the input offset voltage. Since the non-inverting input is at ground, we have

$$V_p = 0 \tag{2}$$

Also, we have

$$V_I = \left(\frac{R_5}{R_4 + R_5}\right) V_{NA} \tag{3}$$

where V_{NA} is the output voltage of the null amp.

Let

$$\frac{R_5}{R_4 + R_5} = p \tag{4}$$

Then, from (1), (2), (3), and (4), we have

$$V_o = A_{vo} (-pV_{NA} - V_{os}) \tag{5}$$

Also, we have

$$V_{NA} = A_{NA} (V_o + V_{osn}) \tag{6}$$

where A_{NA} and V_{osn} are the gain and input offset voltage of the null amp. From (5) and (6) we have

$$V_{NA} = A_{NA} \left[A_{vo} (-pV_{NA} - V_{os}) + V_{osn} \right] \tag{7}$$

which gives

$$V_{NA}\,(1 + A_{NA}A_{vo}p) = A_{NA}\left[\,-A_{vo}V_{os} + V_{osn}\,\right] \tag{8}$$

From the schematic shown in Figure 1, $p = 0.001$, $A_{NA} = 2000$, $2\,A_{vo} >> 1$

Hence:
$$V_{NA} = \frac{2000\left[-A_{vo}V_{os} + V_{osn}\right]}{1 + 2A_{vo}} = -1000\,V_{os} + \frac{1000\,V_{osn}}{A_{vo}} \tag{9}$$

Since the null amp. has a gain of 2000,

$$V_o = \frac{-V_{os}}{2} - V_{osn} \tag{10}$$

Worst case values for the 702 are $A_{vo} = 1500$, $V_{os} = 2\text{mV}$. V_{osn} typically is 2mV. Therefore we have

$$V_{NA} = \left[\,2.000 + \frac{2}{1500}\,\right] \text{ Volts}$$

and

$$V_o = -3\text{mV}$$

If resistor tolerance of ±0.1% were included, V_{NA} would be $1000\,V_{os}$ ±0.3%.

SYM	DESCRIPTION	BY	DATE	APPROVAL

PERFORMANCE BOARD OF DUT

R8, 22M

R11, 10K

C3 .002

R10 10K

K10

20-6

Vcc

AD049-A (NULL AMP)

R9 10K

K9

20-5

R3 22M

R12 470Ω

C4 .002

WORD 55, CHAR 10, BIT 4

WORD 55, CHAR 10, BIT 8 (TO OPEN)

K1 (NORMALLY CLOSED)

R14, 1K

AD027A SAMPLE & HOLD

C1 1μf

CR1

CR2

K2

K3

K5

K6

WORD 58, CHAR 5, BIT 8

R1 50K 0.1%

R2 50K 0.1%

R3 50K 0.1%

R4 50K 0.1%

C5 .01μf

WORD 55, CHAR 10, BIT 1

20-1

R15 2K, 0.1%

K4

R7 50K, 0.1%

K7

20-2

C2 .01μf

R5 50Ω 0.1%

R6 50Ω 0.1%

WORD 55, CHAR 10, BIT 2

K8

20-3

20-4

R16 2K 0.1%

C6 .01μf

C7 .1μf

C8 .1μf

8-1

4-1

7-1

+12V

-6V

2-1

3-1

702 DUT

.01μf

7-3

97020215-04

20-7

17-1

20-8

20-10

20-6

20-9

R19 20K 0.1%

C11 .01μf

C10 .01μf

18-1

R18 100K

R17 2K 0.1%

C9 .01μf

9-1

(UTILITY RELAY)

19-9

19-1

19-10

ITEM NO.	QTY.	PART NUMBER	REF. DES.	DESCRIPTION

REFERENCE DRAWINGS | NEXT ASSY | MDL

MATERIAL

FINISH

TOLERANCES AND NOTES UNLESS OTHERWISE SPECIFIED

DECIMAL .XX ±.010 .XXX ±.005 | FRACTIONAL ±1/64 | ANGULAR ±0°30'

BREAK ALL SHARP EDGES .010
ALL DIMENSIONS INCHES
DO NOT SCALE THIS DRAWING

DRAWN EWING 9-28-67 DATE

CKD DATE

ENGR. DATE

ENGR. DATE

MFG DATE

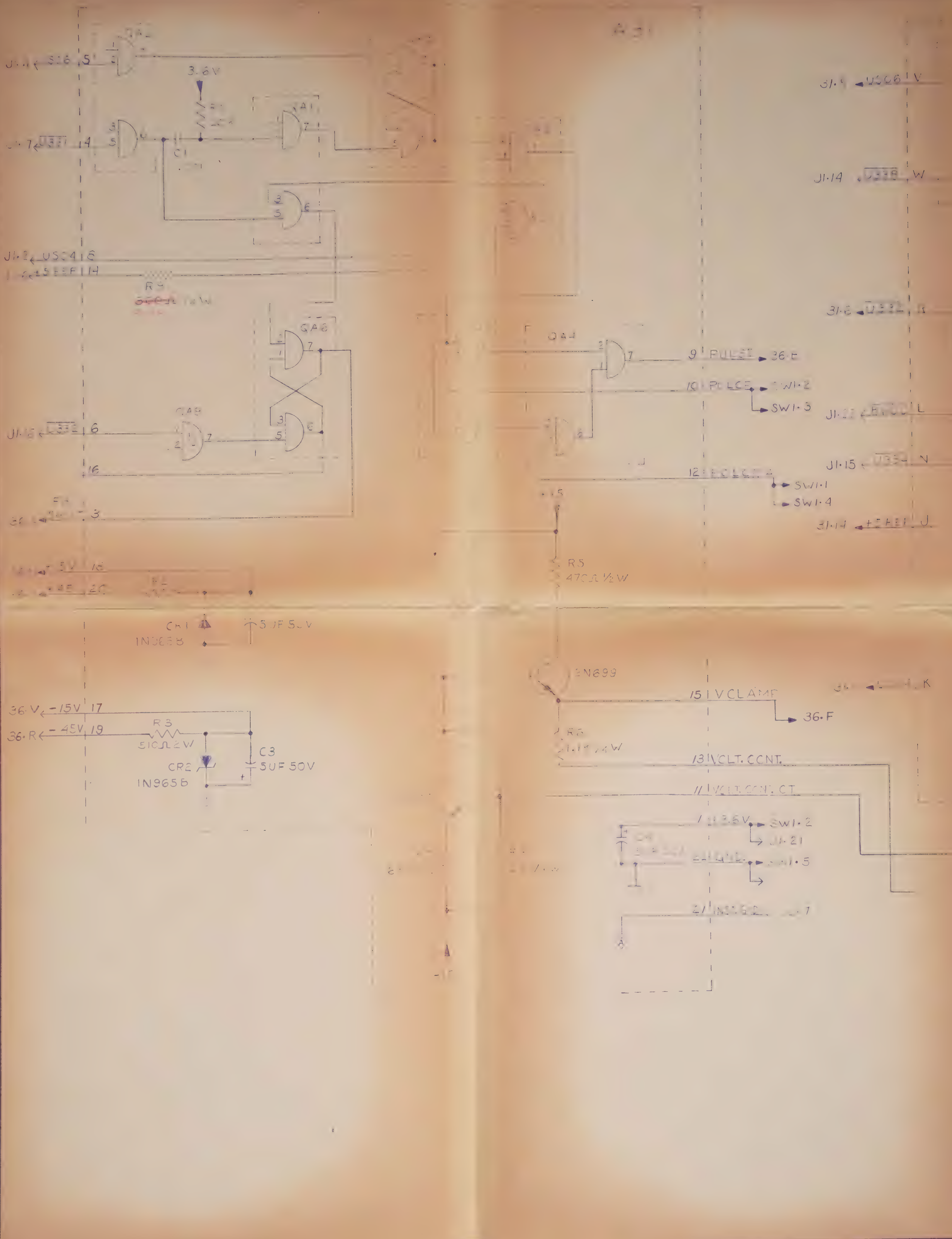
RELEASED DATE

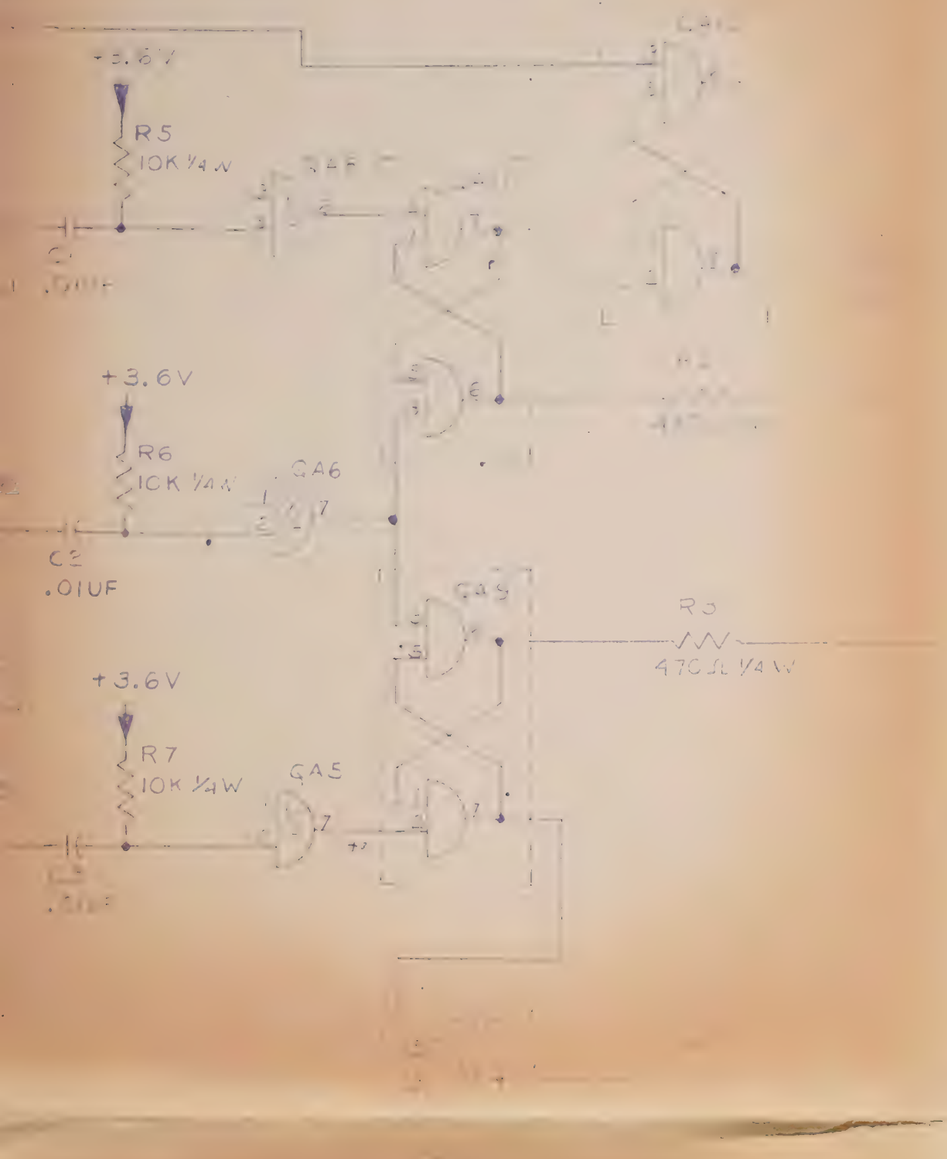
FAIRCHILD INSTRUMENTATION
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

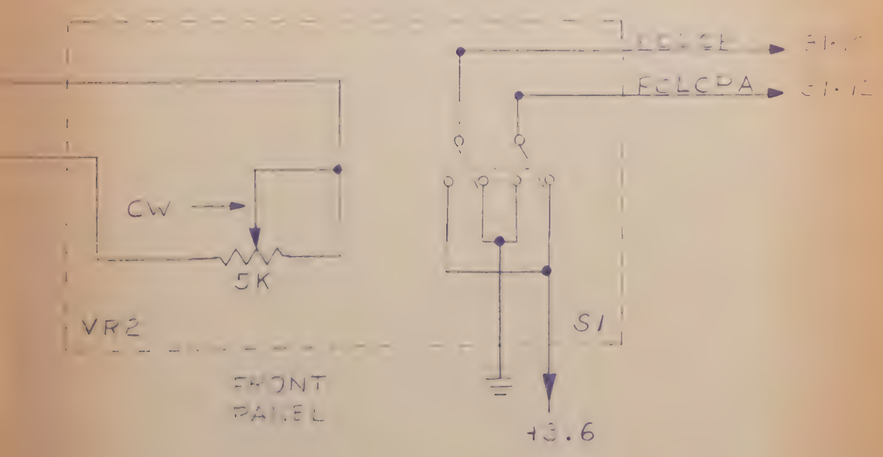
LINEAR CIRCUIT CONTROL CARD

SCALE | DWG. C SIZE | 97020215-04

SHEET OF


3.6V
R1
C1
.01
J1.4 ← S16
J1.7 ← U33F
J1.2 ← USC4
J1.16 ← U33E
R4
1/2W
CR1
IN965B
5UF 5V
36.V ← -15V 17
36.R ← -45V 19
R3
510Ω 2W
CR2
IN965B
C3
5UF 50V
31.9 ← USC6 V
J1.14 ← U33B W
31.E ← U33L R
9 PULSE → 36.E
10 POLCE → SW1.2
SW1.3
J1.15 ← U33H N
12 POLCE A → SW1.1
SW1.4
31.14 ← U33F J
+15
R5
470Ω 1/2W
2N699
15 VCLAMP
36.F
R6
1.1K 1/4W
13 VCLT. CONT.
11 VCLT. CONT. CT
SW1.2
J1.21
SW1.5
21 INSTGD
J1.7
A





ITEM	PART NUMBER	REF DES	DESCRIPTION

REFERENCE DRAWINGS			
NEXT ASSY	USED ON		

DRAWN		DATE
ENGR		DATE
ENGR		DATE
MFG		DATE
QUALITY		DATE

FAIRCHILD
INSTRUMENTATION

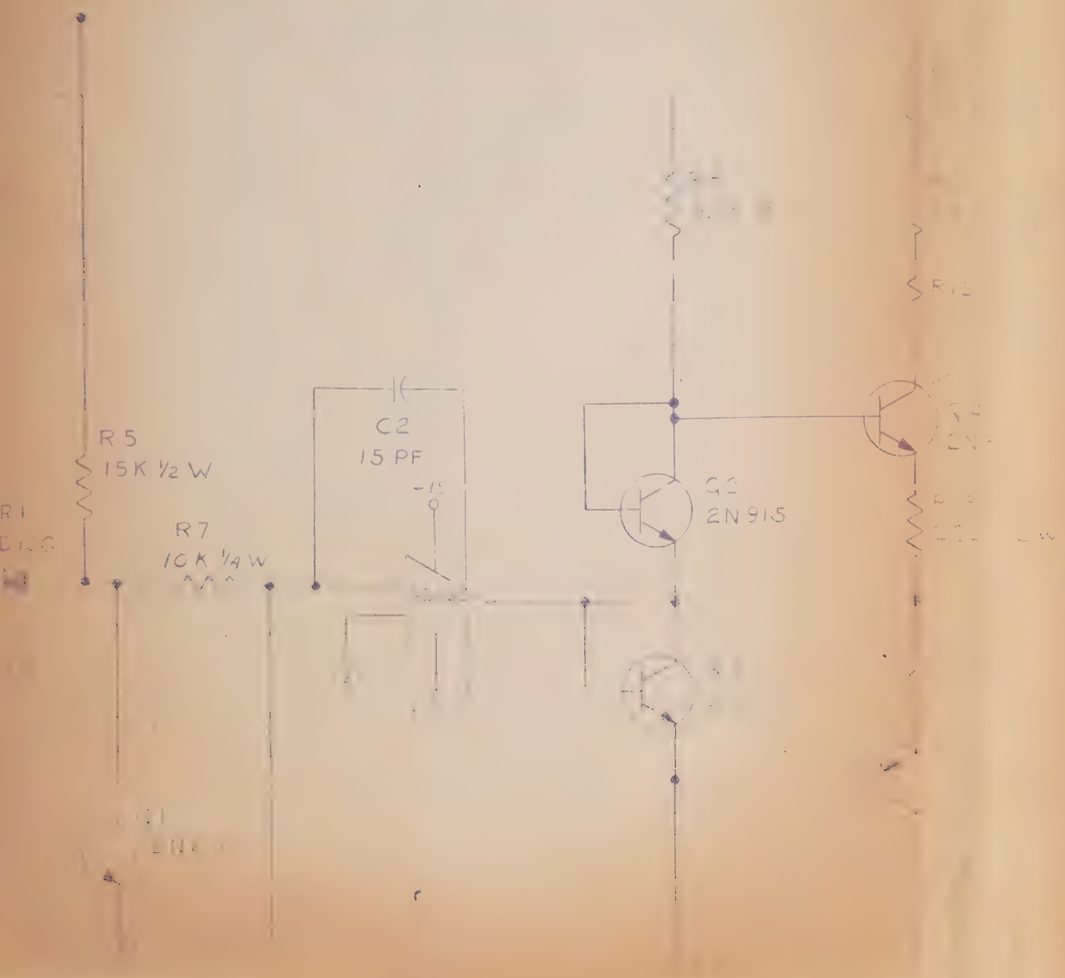
BOEING PULSER
A26 & A31

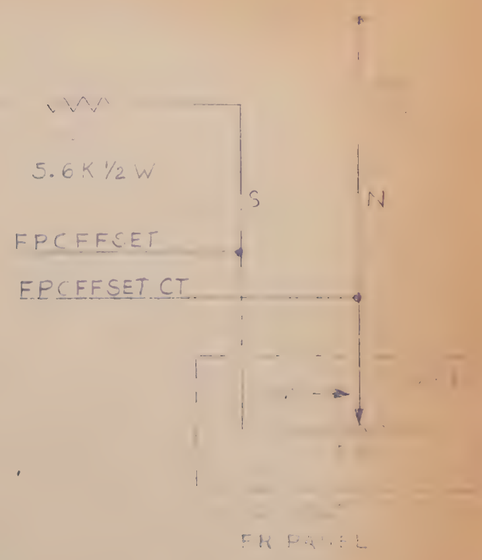
SIZE D | 97047200-04 | REV

SCALE | SHEET 2 OF 2

REVISIONS

SYM	DESCRIPTION	BY	DATE	APPROVED





PART NUMBER	REF DES	DESCRIPTION

FAIRCHILD
INSTRUMENTATION

BOEING PULSE
A 14-30

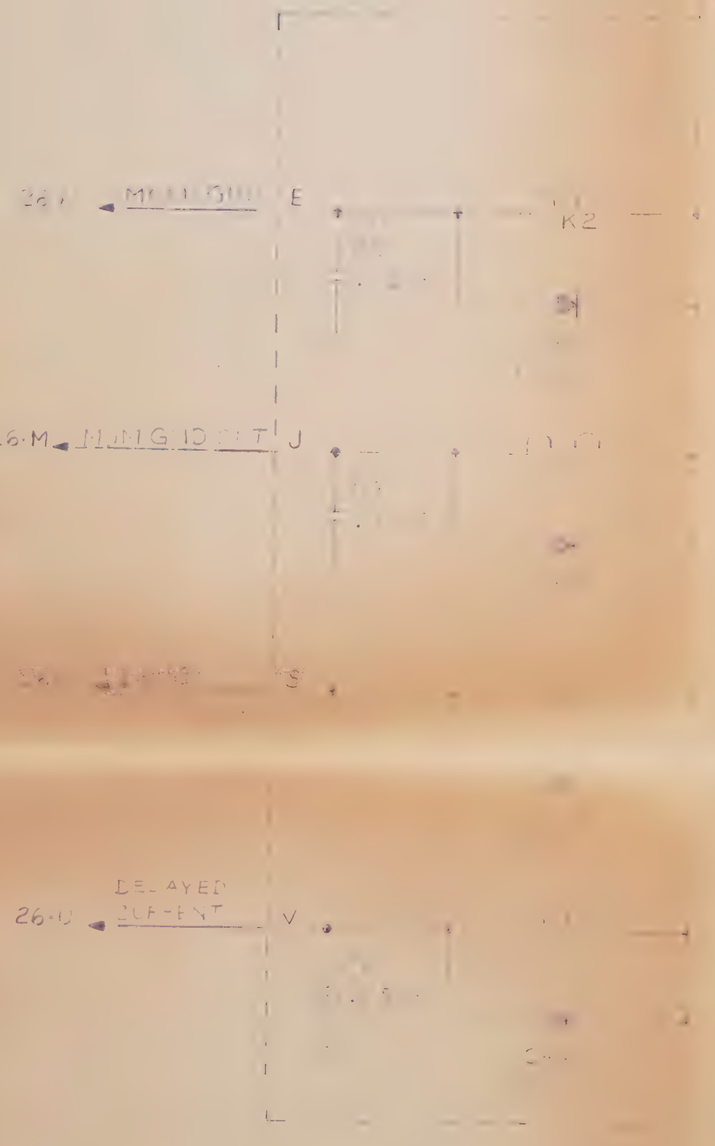
D

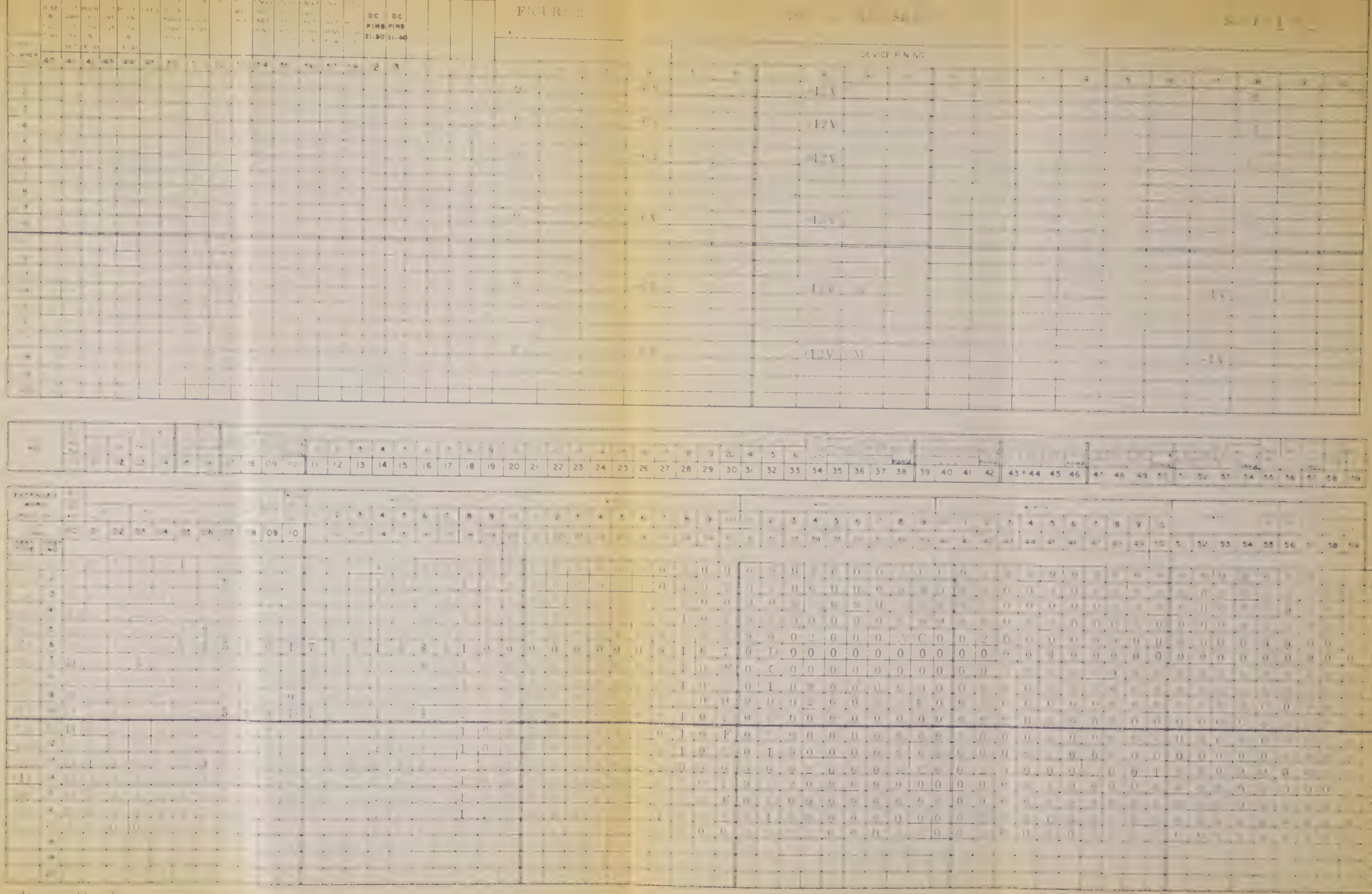
REFERENCE DRAWINGS

NEXT ASSY

SHEET 1

REV


26·J
26·M
K2
K3
.01UF
R3
+EVEN
K
EXT S
31·17
31·15
VCLAMP F
J2·13
U
Y
NOT GATE
DELAYED
CURRENT


DEVICE PIN NO.
+12V
-12V
+5V
-5V
+12V
-12V

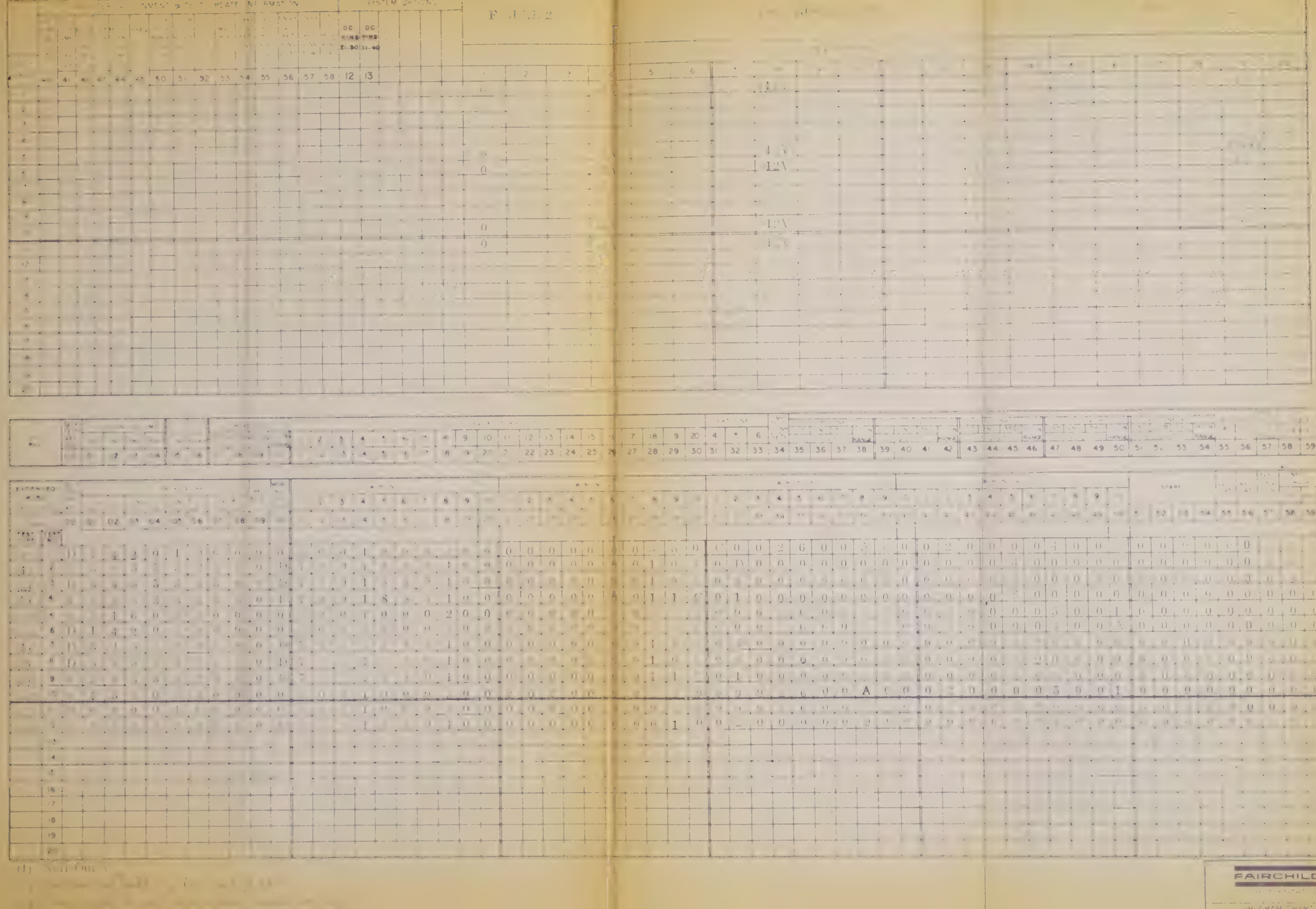


FIGURE 2

702 PROGRAM SHEET

SHEET 3 of 3

REGISTER ASSIGNMENT & TEST UPDATE INFORMATION — SYSTEM OPTIONS

TEST NUMBER	40	41	42	43	44	45	50	51	52	53	54	55	56	57	58	12	13
	PG SEL B FAIL TIME	PS OUT SUP OUT OVR SET	PUL EN STM B DELAY	OUT PUL WID	PULSE LEN STM B DELAY	FREQ	MUX NOISE RANGE START STOP	RANGE DELAY		MAT H/S	SOC RET MINUS	SOC RET PLUS 1-20	SOC RET PLUS 21-30	SOC RET PLUS 31-40	SOC RET PLUS 41-50	DC PINS 21-30	DC PINS 31-60
1																	
2																	
3																	
4																	
5																	
6																	
7																	
8																	
9																	
10																	
11																	
12																	
13																	
14																	
15																	
16																	
17																	
18																	
19																	
20																	

DEVICE PIN NO.

TEST NUMBER	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
1	0			-6V,M				+12V												
2																				
3	0			-6V				+12V,M												
4																				
5	0			-6V				+12V												
6																				
7																				
8	0			-3V				+6V										M		
9	0			-6V				+12V												
10																				
11																				
12	0			-3V				+6V										M		
13	0			-6V				+12V	M								+10V			
14																				
15																				
16																				
17	0			-6V				+12V	M								-10V			
18																				
19																				
20																				

D.C. REG	SELF TEST REG. ADD	D.C. GO/NO GO LIMIT 1ST	2ND	3RD	LEAST	MEAS COND	MEAS RANGE	V MEASURING 1ST	2ND	3RD	PUL B RANGE
	00	01	02	03	04	05	06	07	08	09	10

DEVICE UNDER TEST

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40

EXT LINE

4	5	6
41	42	43

TIME MEAS

34
44

PS LINE 1ST | 2ND | 3RD | PUL B RANGE

35	36	37	38
45	46	47	48

V1 1ST | 2ND | 3RD | V1 RANGE

39	40	41	42
49	50	51	52

V2 1ST | 2ND | 3RD | V2 RANGE

43	44	45	46
53	54	55	56

V3 1ST | 2ND | 3RD | V3 RANGE

47	48	49	50
57	58	59	60

V4 1ST | 2ND | 3RD | V4 RANGE

51	52	53	54
61	62	63	64

PASS CAT	REJ CAT	TEST SEQ ON TRUE	NEXT TRUE IGS	NEXT TRUE UNITS
55	56	57	58	59
65	66	67	68	69

EXTENDED WORD REGISTER	TEST TYPE	TEST NO	SELF TEST REG. ADD	WORD ADDRESS NO1 MS	NO1 LS	NO2 MS	NO2 LS	NO3 MS	NO3 LS	NO4 MS	NO4 LS	REG RESET	WORD NO. SELF TEST
	CHAN NUMBER		00	01	02	03	04	05	06	07	08	09	10

WORD NO.

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40

WORD NO.

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50

WORD NO.

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60

WORD NO.

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90

SPARE				PASS CAT	REJ CAT	TEST SEQ ON TRUE	NEXT TRUE IGS	NEXT TRUE UNITS
91	92	93	94	95	96	97	98	99

| TEST TYPE | TEST NO | | | | | | | | | | | | | | | | | | |

MP MASTER
MA29938